Small Outline Package Guide

1999

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TABLE OF CONTENTS

1

Package Description

CHAPTER 1
PACKAGE DESCRIPTION

1.1. INTRODUCTION

Throughout the electronics industry, a worldwide push towards increased mobility, lower power, and higher functionality is placing higher demands on semiconductor devices. Today's form factor driven requirements are leading to new breeds of fine pitch integrated circuit packages. Currently, submicron feature size at the die level are driving package feature sizes down to the design-rule level of the early technologies. To meet these demands, package technology must deliver higher lead counts, reduced lead pitch, minimum footprint area, and significant overall volume reduction.

The Plastic Small Outline Package (PSOP), Thin Small Outline Package (TSOP), and Shrink Small Outline Package (SSOP) are the surface mount memory packaging from Intel. These Small Outline Packages give users strong packaging choices for all types of applications. In addition they support the widest range of nonvolatile memory component densities and features for the user's applications.

Key features of the Plastic Small Outline Package (PSOP) include:

- JEDEC standard compliance
- Footprint and height 50% of DIP
- Two side leaded for routing simplicity
- 50 mil (1.27 mm) pitch for SMT simplicity and ease of use
- Gull wing formed leads for improved SMT manufacturing
- Supports future flash density and feature growth
- Outstanding in any temperature application

Key features of the Thin Small Outline Package (TSOP) include:

- JEDEC and EIAJ standard dimensions
- Smallest leaded package from factor for flash
- 0.5 mm (19.7 mil) lead pitch
- Reduced total package height, 1.20 mm maximum
- Gull wing formed leads for improved SMT manufacturing
- Supports future flash density and feature growth

Key features of the Shrink Small Outline Package (SSOP) include:

- JEDEC standard compliance
- Direction for Intel's higher density flash architectures
- 0.8 mm (31.5 mil) lead pitch offers handling characteristics similar to 50 mil pitch packages
- Excellent performance in wide temperature applications
- Two sided and gull wing lead package design

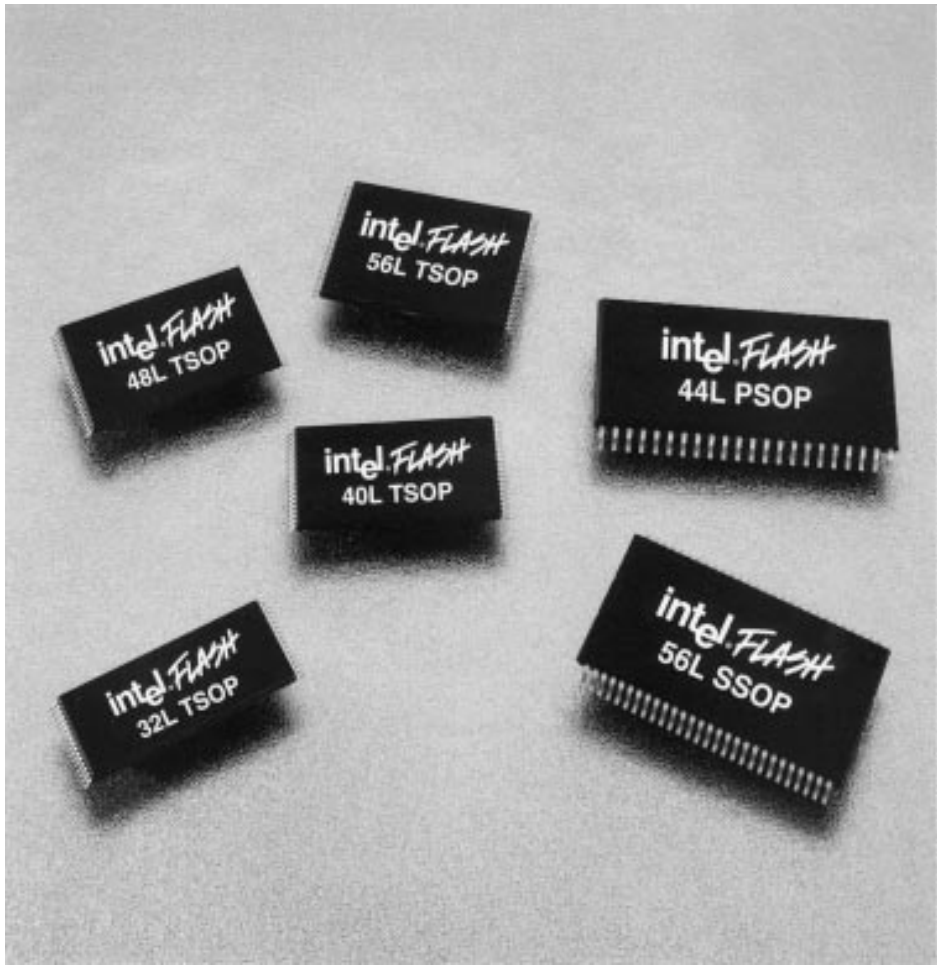

Figure 1-1. Intel's Flash Memory Small Outline Family

1.2. PACKAGE INFORMATION

The TSOP package is offered in 32-lead, 40-lead, 48-lead and 56-lead versions in JEDEC and EIAJ registered standard dimensions. The PSOP and SSOP are JEDEC standard compliant.

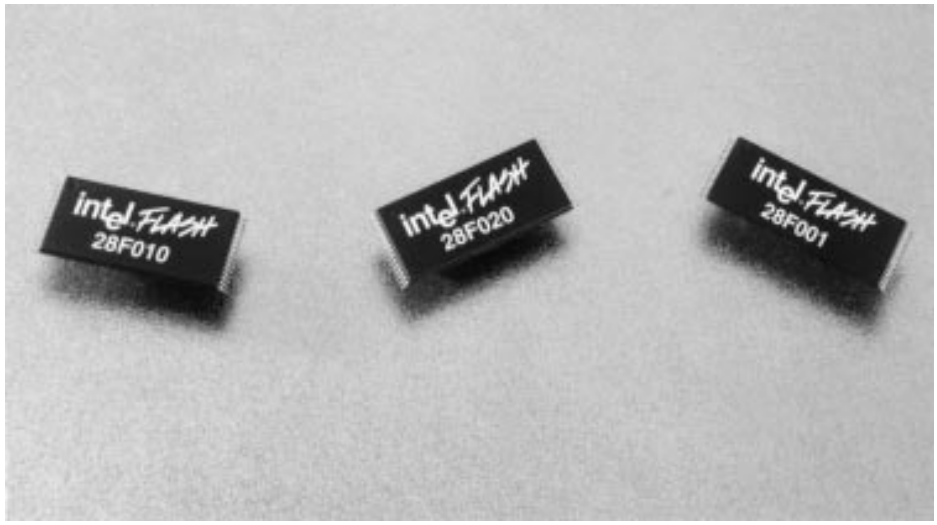

Figure 1-2. 32-Lead TSOP Package

Intel's 32-lead TSOP package accommodates Intel's first generation, the 28F010 1-megabit and 28F020 2-megabit flash memory devices, in an EPROM-compatible pinout with an easy single pin density upgrade path. The 28F001BX 1-megabit Boot Block flash memory is also available in the 32-lead TSOP package.

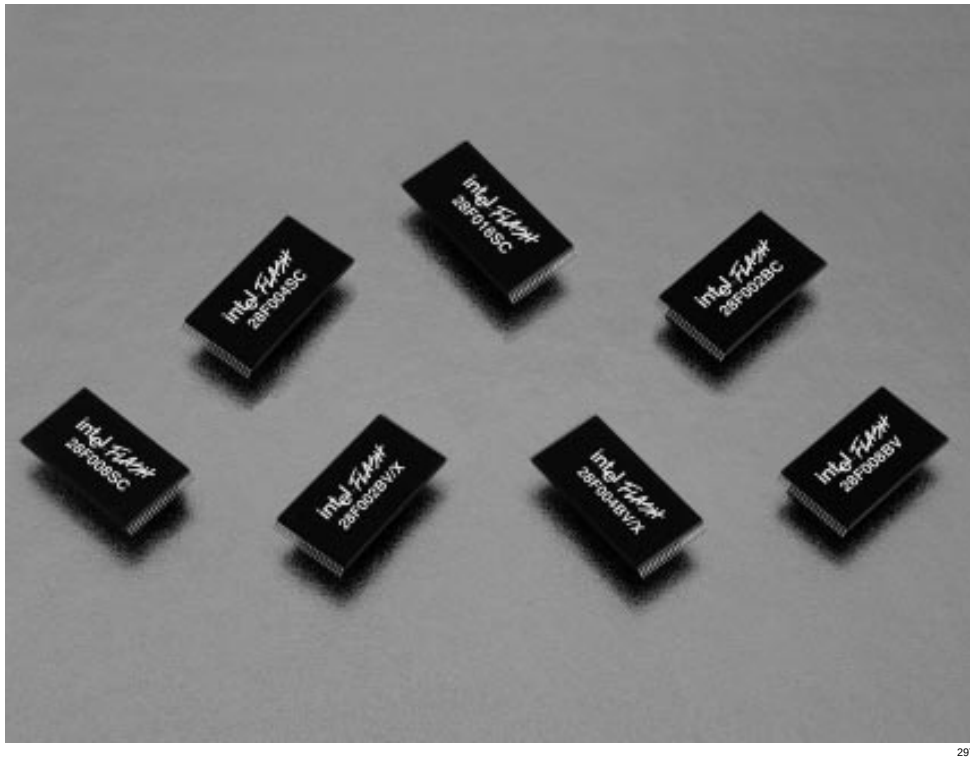

Figure 1-3. 40-Lead TSOP Package

Intel's 28F004SC 4-megabit, 28F008SC 8-megabit and 28F016SC 16-megabit FlashFile™ memories are offered in a 40-lead TSOP. The 28F002BV/X 2-megabit, 28F004BV/X 4-megabit and 28F008BV 8-megabit Boot Block Flash memories are also offered in the 40-lead TSOP package. The FlashFile products support an easy single pin upgrade path from the 4-megabit density to the 16-megabit density. The Boot Block products support a similar upgrade path from the 2-megabit density to the 8-megabit density. The package pin count also allows for the implementation of Intel's SmartVoltage architecture. This is designed in the SC FlashFile components and the BV Boot Block components. This gives the user the choice of low power read, single 5V operation or 12V high speed programming and erase. In addition, Intel's 28F002BC 2-megabit memory is offered in the 40-lead TSOP.

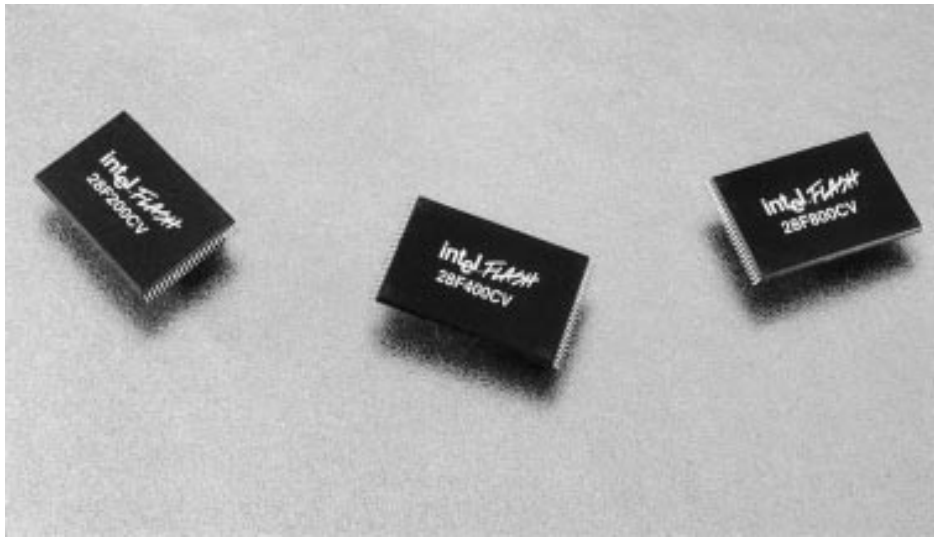

Figure 1-4. 48-Lead TSOP Package

Intel's 48-lead TSOP package is Intel's latest offering in extremely small form factor packaging. Intel's 28F200CV 2-megabit, 28F400CV 4-megabit and 28F800CV 8-megabit Boot Block Flash memories are offered in the 48-lead TSOP package. Like 40-lead TSOP there is an easy pinout upgrade path from the 2-megabit Book Block to 4-megabit Boot Block density and from the 4-megabit Boot Block to the 8-megabit Boot Block Density. The 48-lead Boot Block components allow the user to configure in a x8 or x16 organization and has Intel's SmartVoltage technology.

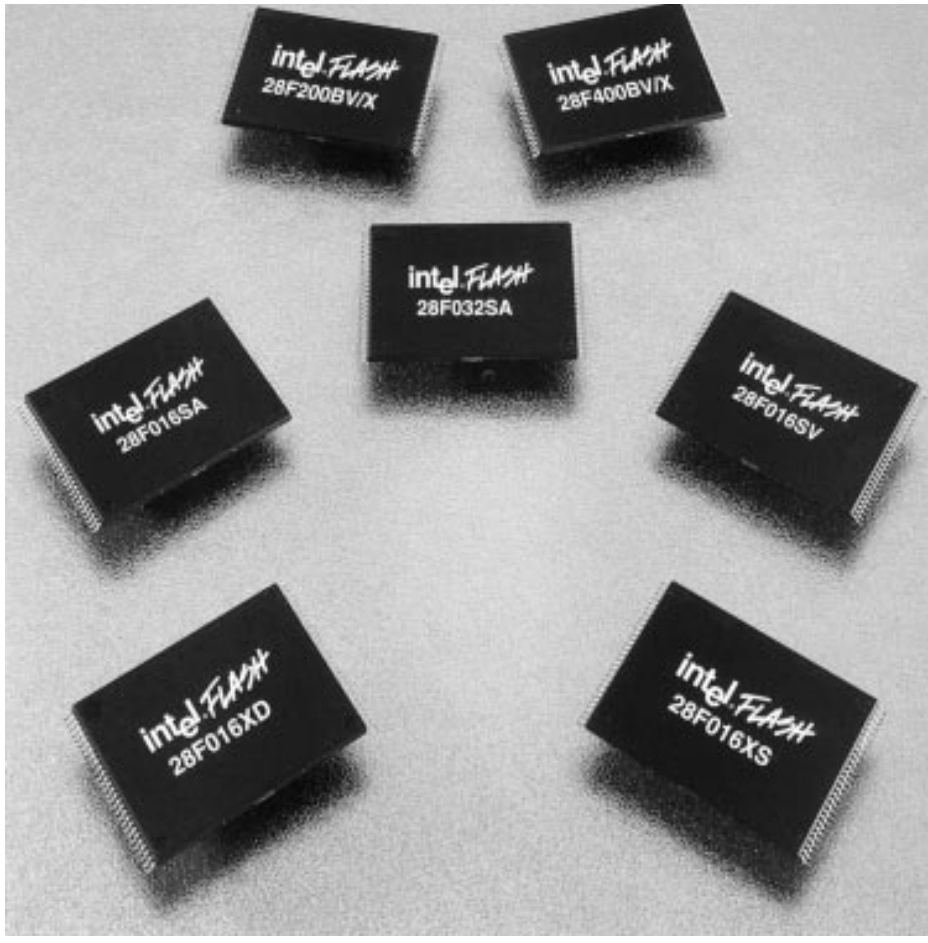

Figure 1-5. 56-Lead TSOP Package

The 56-lead TSOP pinout allows for a user configurable x8 or x16 organization in a small form factor, and offers room to grow as memory density and features dictate. Intel's 28F200BV[1] and BX 2-megabit and 28F400BV[1] and BX 4-megabit Boot Block Flash memories are offered in the 56-lead TSOP package. In addition Intel's higher density products also are offered in a 56-lead TSOP package. They include the 28F016SA and 28F016SV[1] 16-megabit FlashFile memories and the DD28F032SA 32-megabit FlashFile memory. The DD28F032SA is the result of an advanced packaging innovation that encapsulates two 28F016SA die in a single Dual Die Thin Small Outline Package (DDTSOP). Intel's latest offering in 56-lead TSOP are the 28F016XD (x16 architecture only) and 28F016XS[1].

These two devices are part of Intel's High Performance family and were designed with optimized system interfaces. The XD device offers a DRAM interface, while the XS device offers a synchronous interface.

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[1] SmartVoltage technology

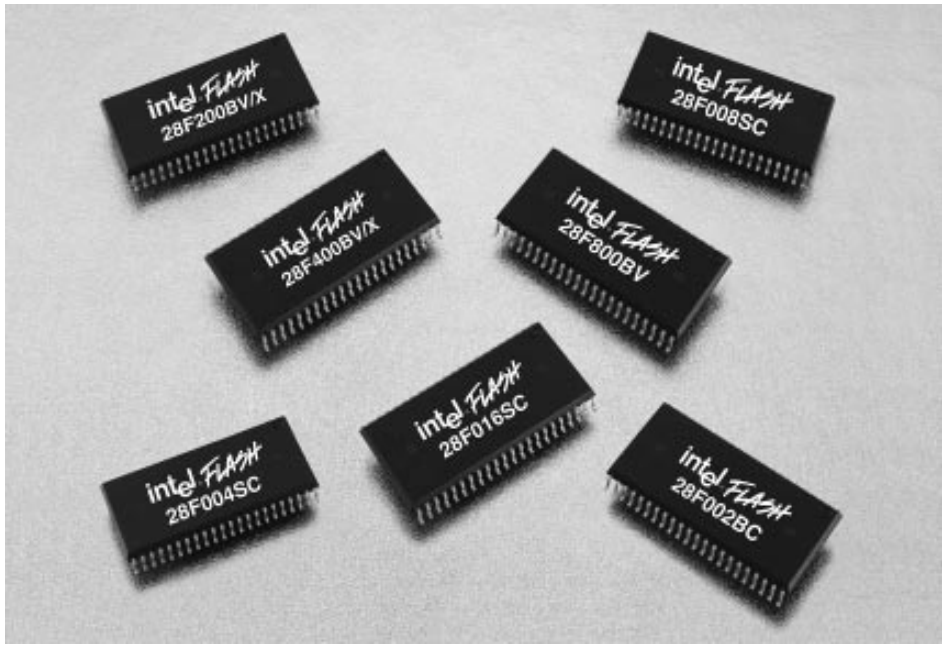

Figure 1-6. 44-Lead PSOP Package

The 44-lead PSOP dimensions are a registered JEDEC standard. Intel's 28F004SC 4-megabit, 28F008SC 8-megabit and 28F016SC 16-megabit FlashFile memories are offered in the 44-lead PSOP. The 28F200BV/X 2-megabit, 28F400BV/X 4-megabit and 28F800BV 8-megabit Boot Block flash memories are also offered in the 44-lead PSOP. The Boot Block flash memories feature a ROM-compatible pinout in a user configurable x8 or x16 organization. The 28F002BC 2-megabit memory is also offered in the 44-lead PSOP.

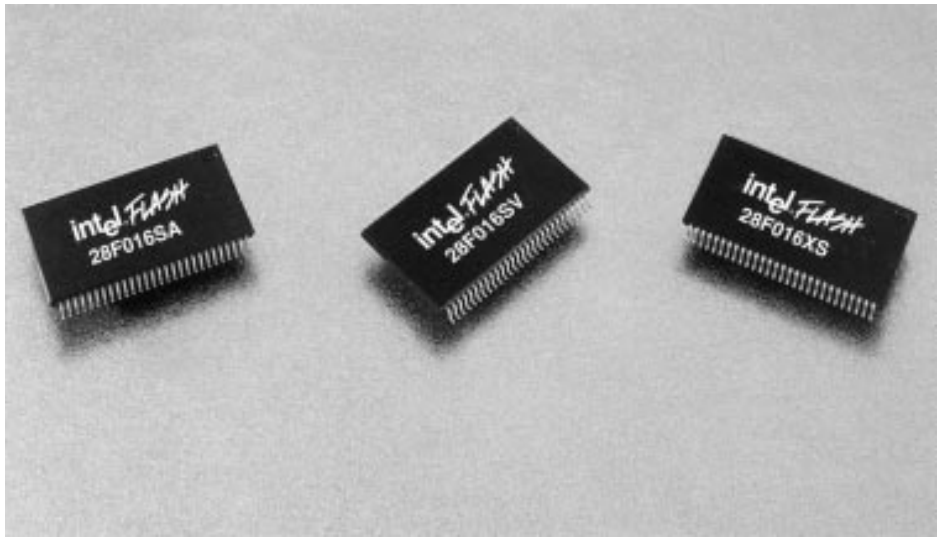

Figure 1-7. 56-Lead SSOP Package

The 56-lead SSOP is a recent SOP offering from Intel. The package dimensions are in compliance with JEDEC standards. The SSOP is the direction for Intel's higher density flash architectures in high reliability applications. Intel currently offers the 28F016SA and has plans to put the 28F016SV[2] 16-megabit FlashFile and the 28F016XS[2] 16-megabit Embedded Flash RAM in the package.

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[2] SmartVoltage technology

2

SOP Layout Features and Applications

CHAPTER 2
SOP LAYOUT FEATURES AND APPLICATIONS

2.1. SOP SPACE SAVING FEATURES

The PSOP (Plastic Small Outline Package), SSOP (Shrink Small Outline Package), and TSOP (Thin Small Outline Package) offer several features that minimize the total volume consumed by memory components in a system design. The 1.2 mm thickness of the TSOP is one-third to one-half that of the SOICs, SOJs and PLCCs. The TSOP package's two sided pinouts and standard/reverse pinout offerings minimize both board area and circuit board layers consumed by memory. The 2.80 mm thickness of the PSOP and 1.80 mm thickness of the SSOP are less than half that of standard Plastic DIP (PDIP) packages.

The PSOP and SSOP feature 1.27 mm (50 mil) and 0.8 mm pitch gull wing leads respectively. The leads on the PSOP and SSOP are located on the two long sides of the package. The TSOP features 0.5 mm pitch gull wing leads located on the two short sides of the package. Positioning the leads in this manner leaves two sides of the package open. The open sides of the package can be used to route traces under the component, thus saving board layers and simplifying board layout. Because the leads are on two sides of the package rather than four, all three packages can be placed much closer to each other and to other components on the board.

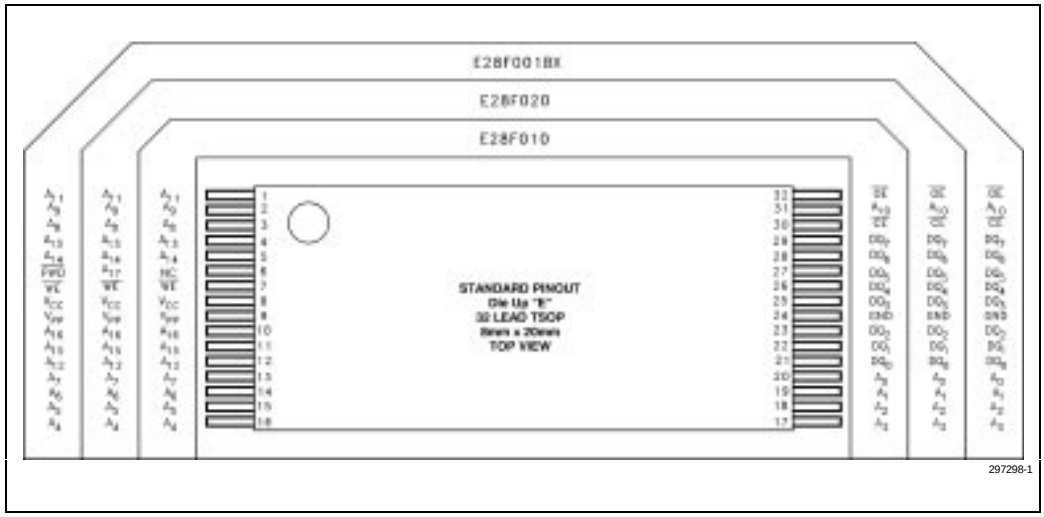


Figure 2-1. 32-Lead TSOP Package Pinout for 28F001BX, 28F010 and 28F020—Standard Pinout

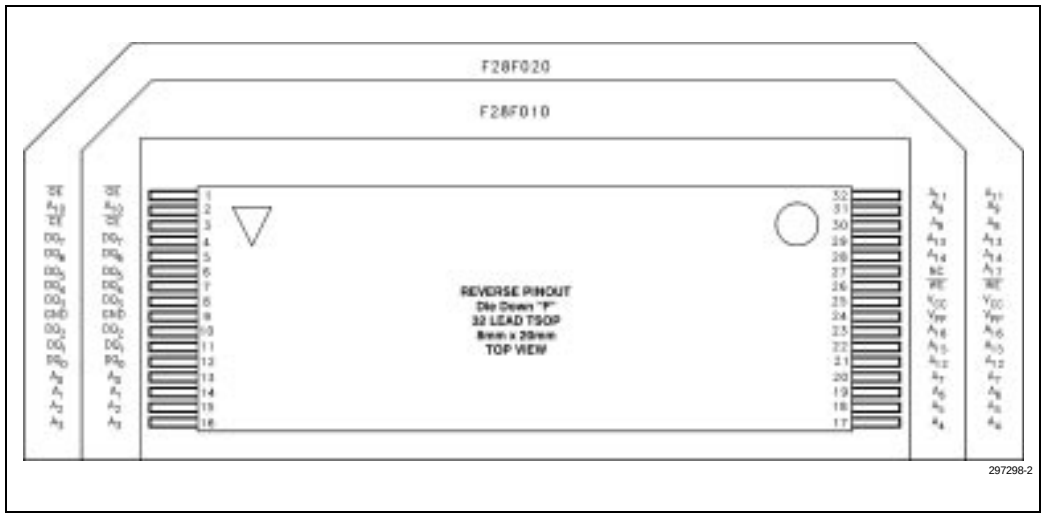


Figure 2-2. 32-Lead TSOP Package Pinout for 28F001BX, 28F010 and 28F020—Reverse Pinout

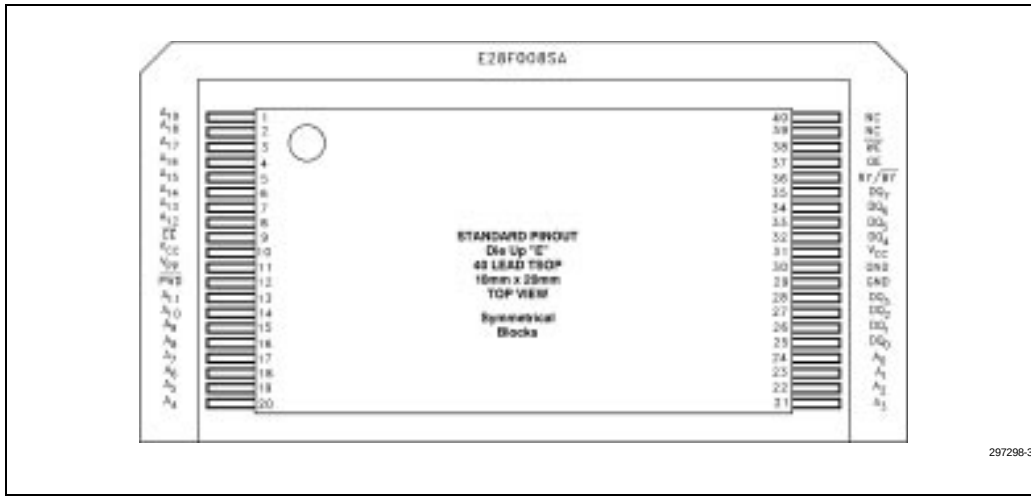


Figure 2-3. 40-Lead TSOP Package Pinout for 28F008SA—Standard Pinout

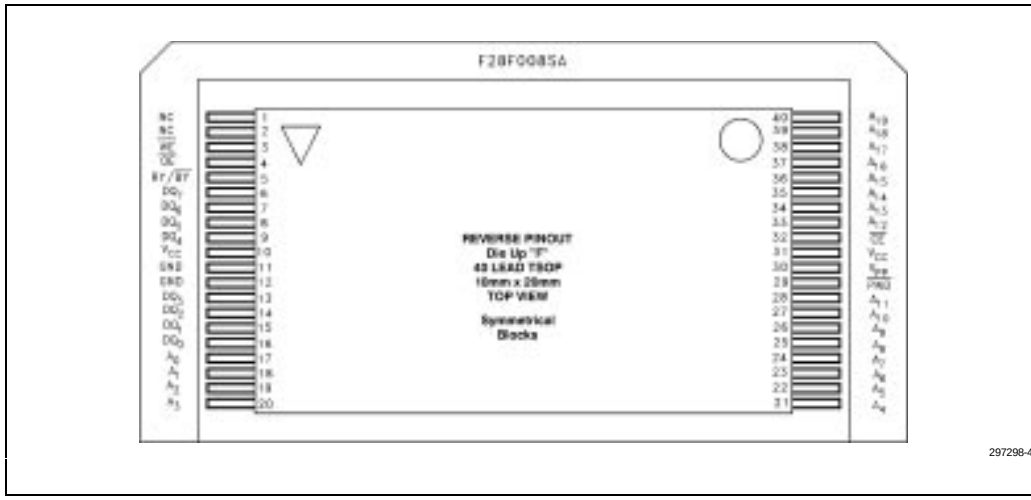
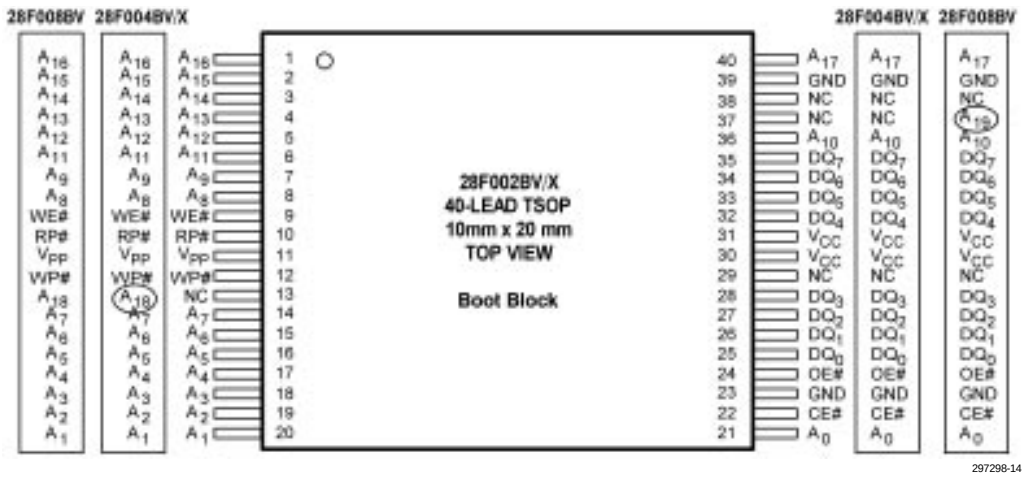


Figure 2-4. 40-Lead TSOP Package Pinout for 28F008SA—Reverse Pinout



NOTE:

Pinout above is SmartVoltage BV version.
Pin 12 is DU for BX/BL 12V V_{PP} versions.

Figure 2-5. The 40-Lead TSOP Pinout for 28F002BV and BX, 28F004BV and BX, and 28F008BV

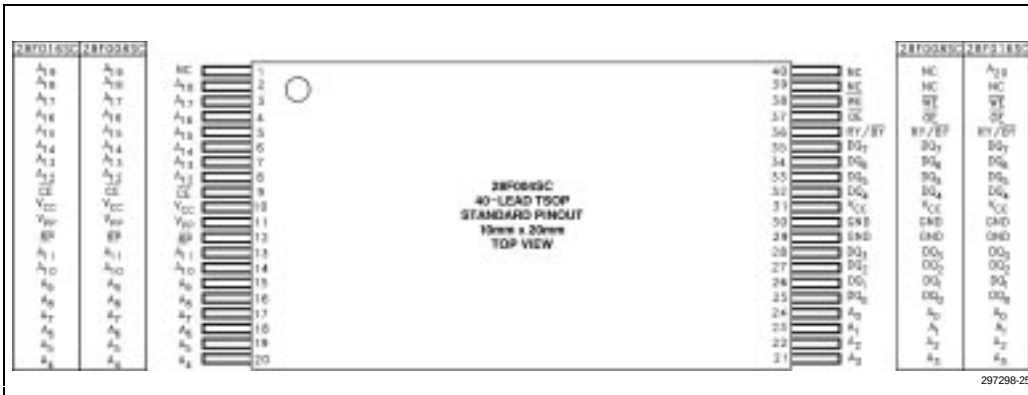


Figure 2-6. The 40-Lead TSOP Pinout for 28F004SC, 28F008SC, and 28F016SC

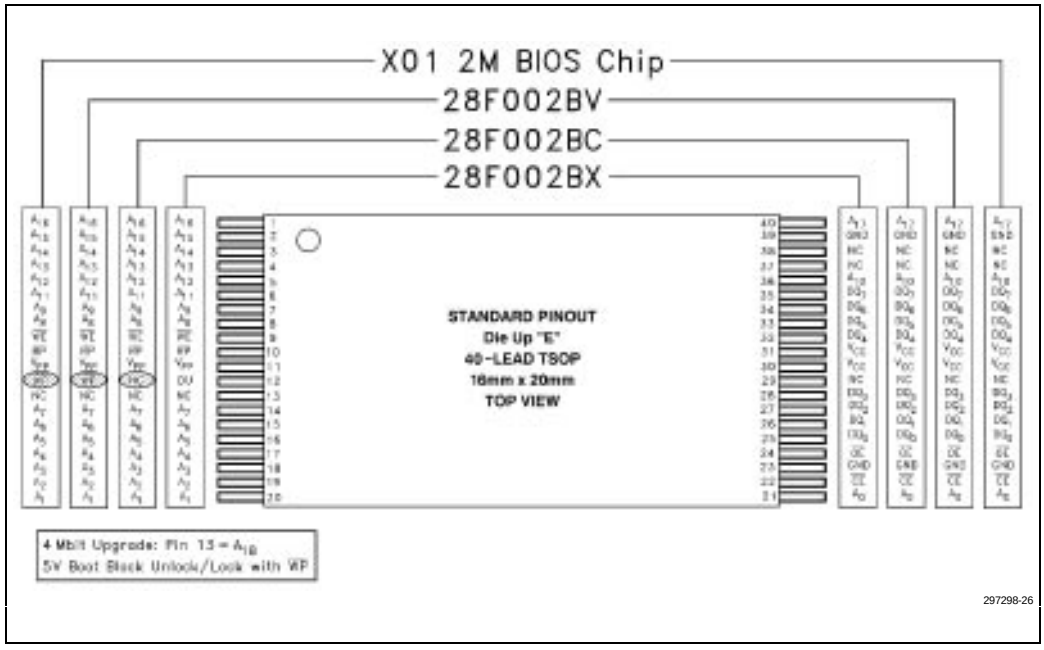


Figure 2-7. The 40-Lead TSOP Pinout for X01 2M BIOS, 28F002BV, 28F002BC, and 28F002BX

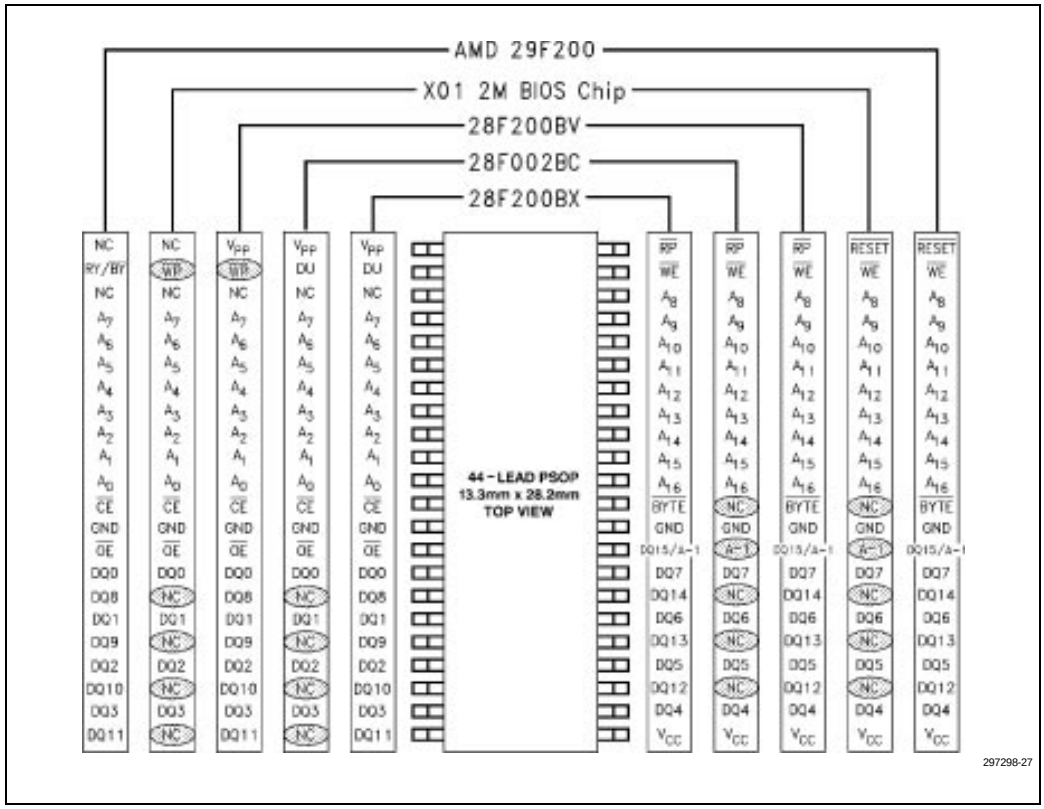


Figure 2-8. The 44-Lead PSOP Pinout for X01 2M BIOS Chip, 28F200BV, 28F002BC, 28F200BX vs. AMD 29F200

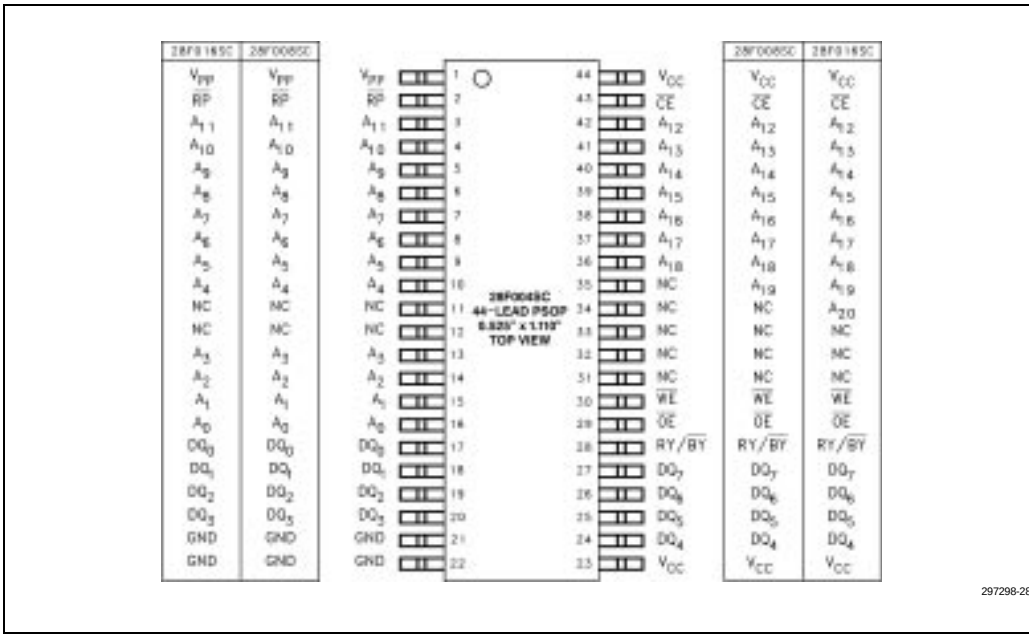
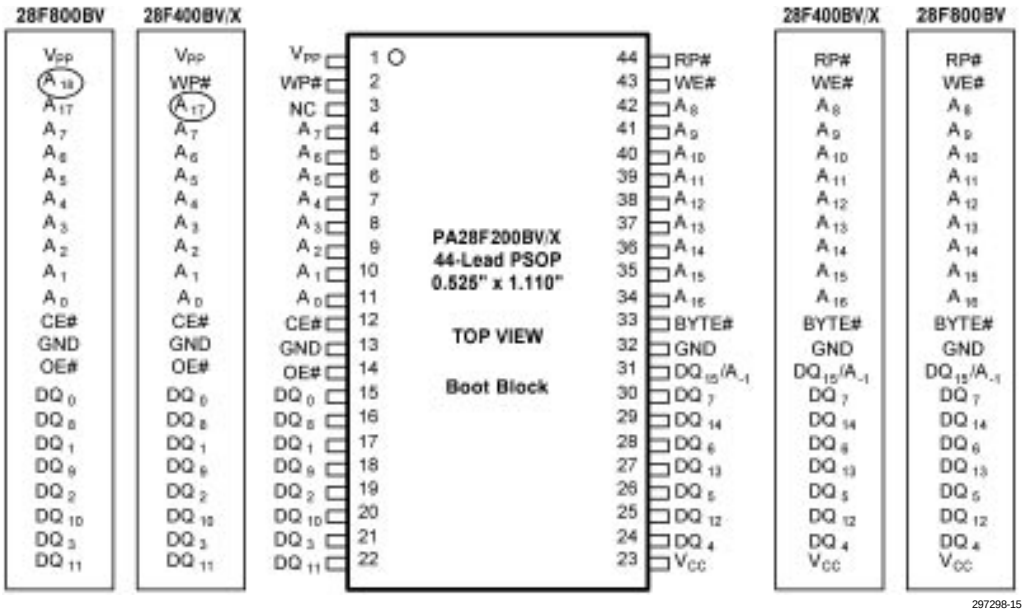


Figure 2-9. The 44-Lead PSOP Pinout for 28F004SC, 28F008SC, and 28F016SC



NOTE:

Pinout above is SmartVoltage BV version.
Pin 2 is DU for BX/BL 12V V_{PP} versions, but for the 8-Mbit device, pin 2 has been changed to A_{18} (WP# on 2/4 Mbit). Designs planning on upgrading to the 8-Mbit density from the 2/4-Mbit density in this package should design pin 2 to control WP# functionality at the 2/4-Mbit level and allow for pin 2 to control A_{18} after upgrading to the 8-Mbit density.

Figure 2-10. The 44-Lead PSOP Pinout for 28F200BV and BX, 28F400BV and BX, and 28F800BV

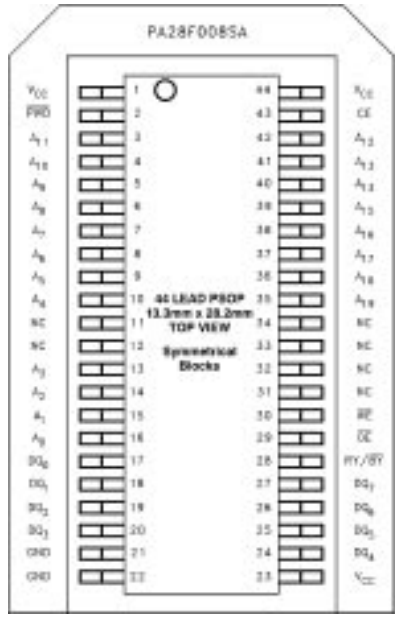
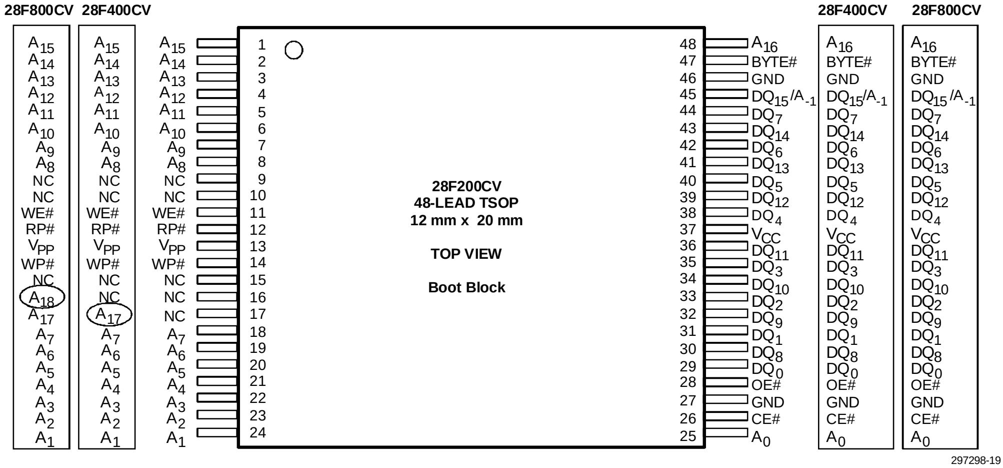


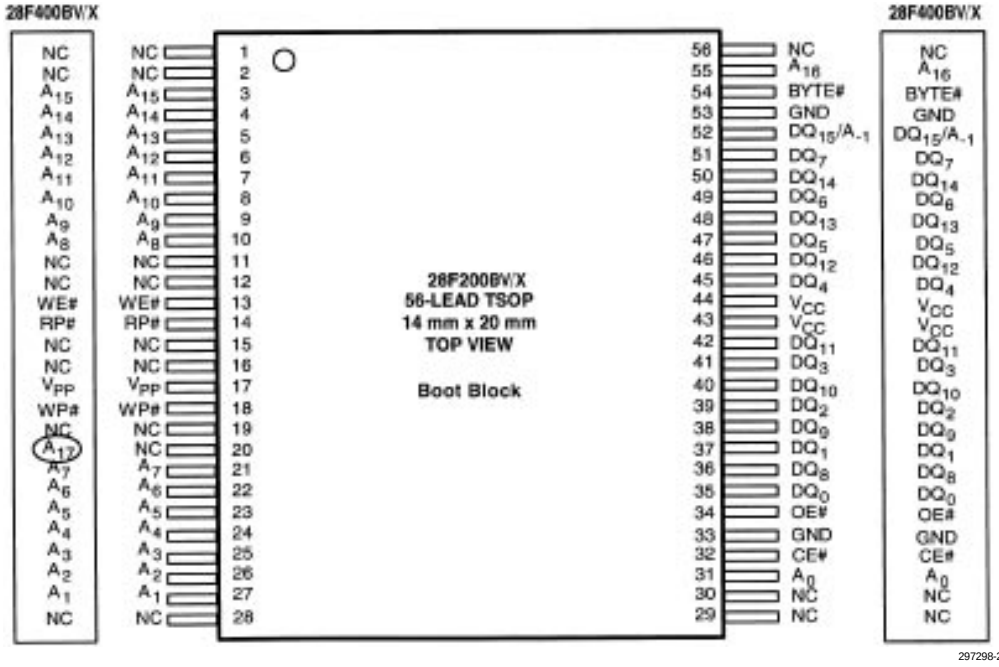
Figure 2-11. 44-Lead PSOP Package Pinout for 28F008SA



NOTE:

CV Pinout is SmartVoltage technology.

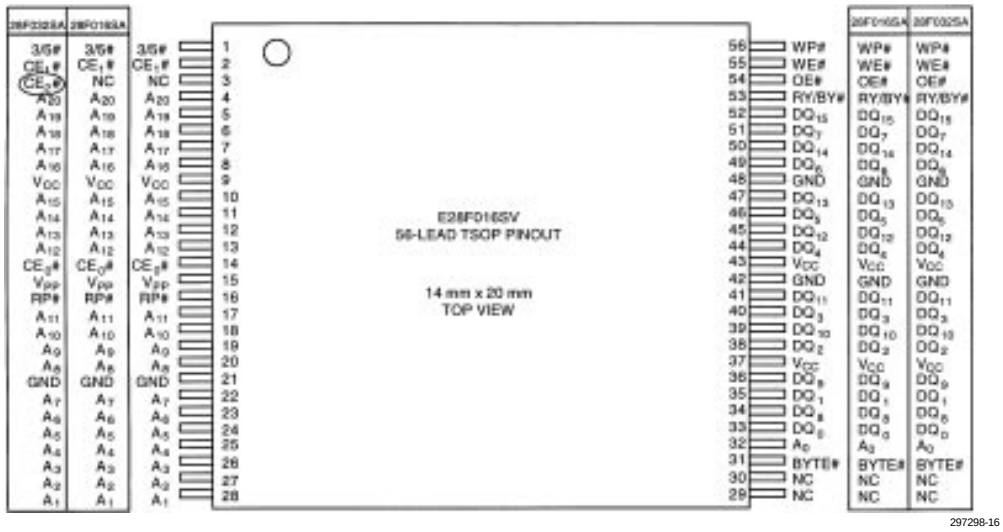
Figure 2-12. The 48-Lead TSOP Pinout for 28F200CV, 28F400CV and 28F800CV



NOTE:

Pinout above is SmartVoltage BV version.
Pin 18 is DU for BX/BL 12V V_{PP} versions.

Figure 2-13. The 56-Lead TSOP Pinout for 28F200BV and BX, and 28F400BV and BX



NOTE:
E28F016SV is SmartVoltage technology.

Figure 2-14. 28F016SV 56-Lead TSOP Pinout Configuration Shows Compatibility with 28F016SA/28F032SA

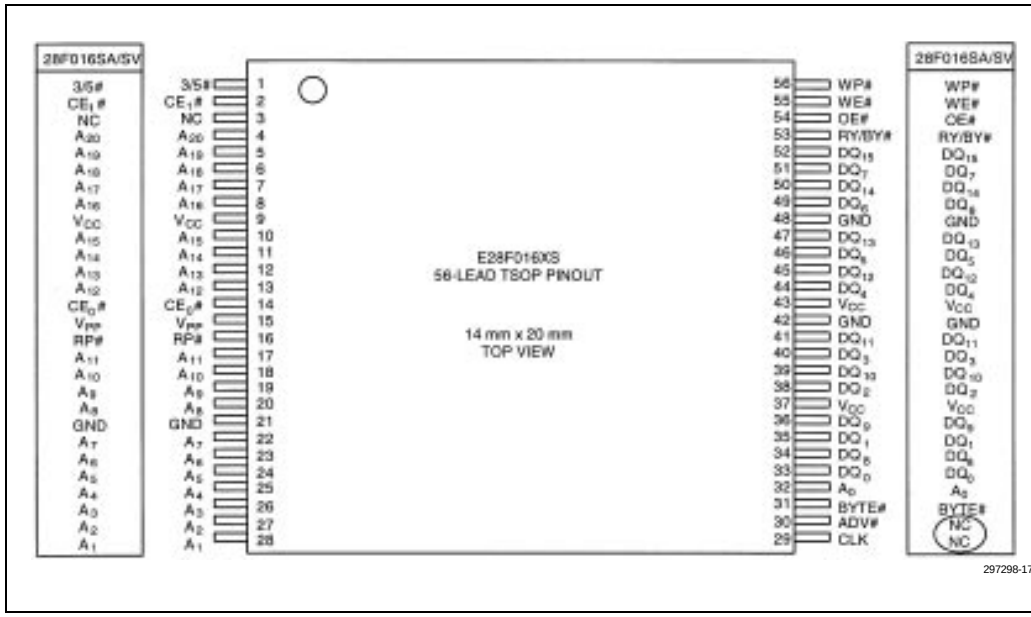


Figure 2-15. 28F016XS 56-Lead TSOP Pinout Configuration Shows Compatibility with the 28F016SA/SV, Allowing for Easy Performance Upgrades from Existing 16-Mbit Designs

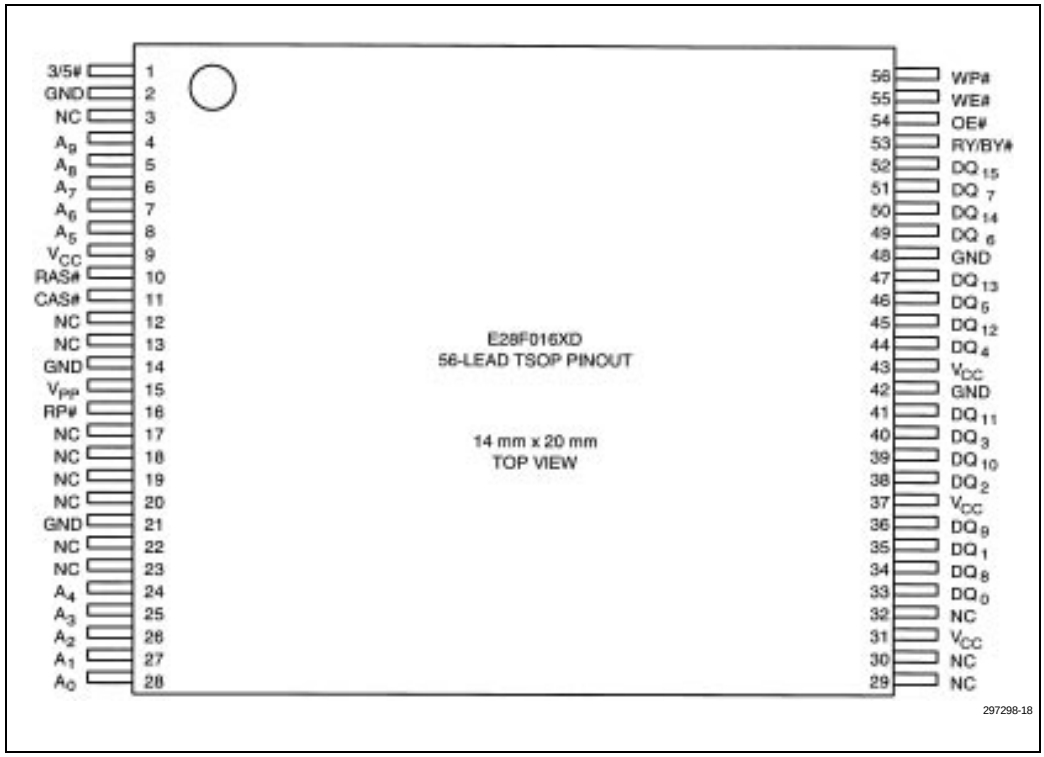
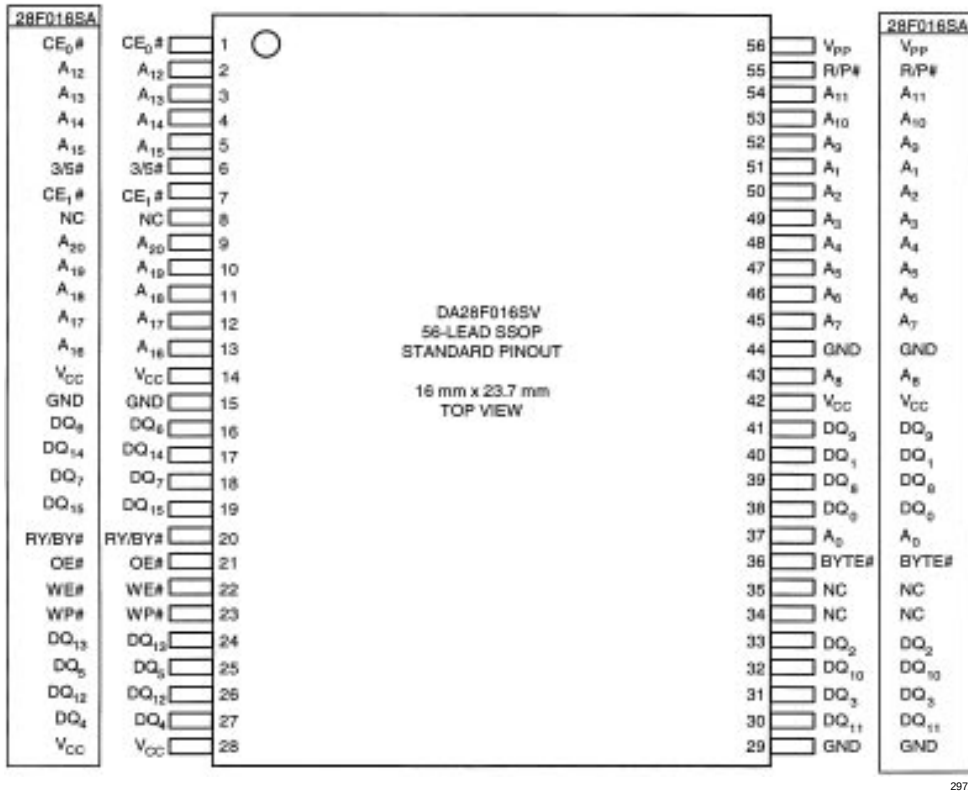


Figure 2-16. 28F016XD 56-Lead TSOP Type I Pinout Configuration



NOTE:
DA28F016SV is SmartVoltage technology.

Figure 2-17. 56-Lead SSOP Pinout Configuration

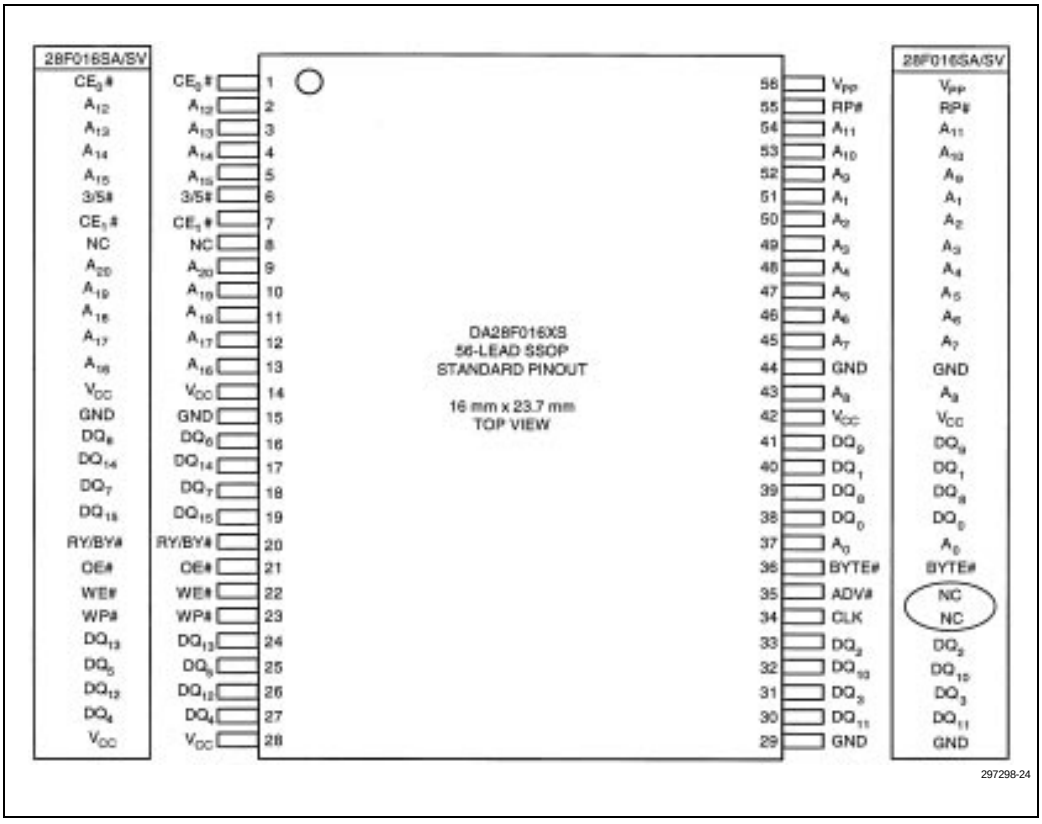


Figure 2-18. 28F016XS 56-Lead SSOP Pinout Configuration Shows Compatibility with the 28F016SA/SV, Allowing for Easy Performance Upgrades from Existing 16-Mbit Designs

2.2. SOP APPLICATIONS

SOP packages support the trend toward miniaturization by consuming one-third to one-half the volume of earlier packaging alternatives. SOP components are a logical choice for the small form factor of handheld instruments, portable communication devices, laptop and notebook PCs, disk drives, and numerous other applications.

In particular, TSOP components can be used to maximize the memory packing density for a given volume constraint. This extra memory can expand the amount of data collected in data acquisition applications or add density to solid state code storage in embedded control, data files and reprogrammable environments. An excellent example is the storage of embedded firmware or application code on a flash-based solid state disk drive or in resident flash memory arrays. The use of flash memory enhances product performance by eliminating the slow, power hungry disk to DRAM software down-loads, thereby decreasing system power up and response time and increasing battery life.

Intel's TSOP packages open up a number of applications. One example is the memory card. The 1.2 mm package height of the TSOP package allows the packing of a board with TSOP devices mounted on both sides with the 3.3 mm PCMCIA/JEIDA standard memory card thickness. Many of Intel's flash architectures are also offered in die form in Intel's SmartDie™ family of products. The SmartDie products allow for direct chip attachment. Intel's flash components in TSOP package and Intel's flash products in the SmartDie family see a complete test flow prior to board mounting. Complete product testing prior to assembly allows arrays of devices to be mounted with predictable reliability and manufacturing yields.

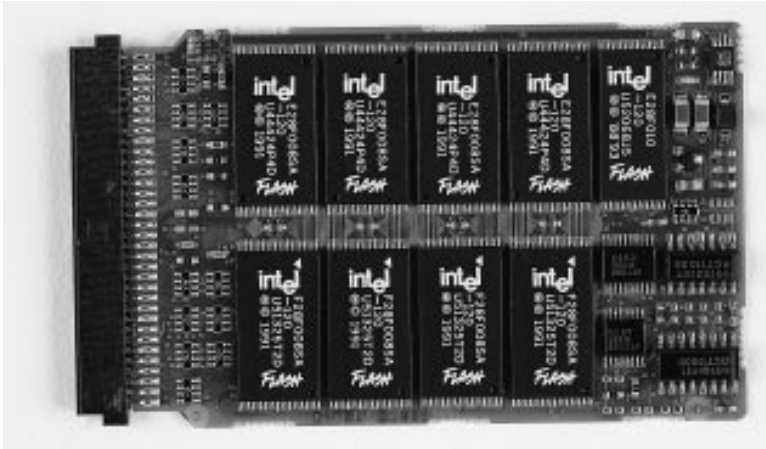


Figure 2-19. TSOP Is Ideal for Memory Card Applications

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Figure 2-20. TSOP Enables New Form Factor Designs and New Innovations

Intel components in PSOP are ideally suited for a number of areas and in particular work well in environments that currently use the PLCC package in applications. User benefits include increased flexibility. This is a result of present and future densities and features that the PSOP enables. Intel's Boot Block architecture is available in PSOP which features Intel's SmartVoltage technology. This allows the user to choose low power 3.3V read, 5V only operation, or high speed programming or erase with 12V. The 12V option is ideally suited for users who pre-program the component prior to assembly. The faster programming capability saves time and equipment in manufacturing. The PSOP's 50 mil lead pitch also allows the user to make an easy transition to SOP. The package is easily adopted in today's 50 mil programming and board assembly environment that supports PLCC. In particular PSOP is a good choice for office automation, industrial control, networking and consumer applications. PSOP pitch and lead height make it an excellent choice for any application that will be exposed to a wide or even extreme temperature condition. Likewise SSOP with its 0.8 mm pitch and similar lead height to PSOP makes it perform similar to PSOP and PLCC. SSOP is the high reliability package direction for Intel's higher density architectures and is an excellent choice in applications that will be exposed to a wide range of temperature conditions. SSOP can be easily implemented into the 50 mil pitch assembly environment. One other SOP benefit for assembly is the package's gull wing leads. The exposed lead design allows for easier inspection of the leads solder joints.

Figure 2-21. PSOP Is Easy to Implement and Enables Unique Capabilities

3

SOP Physical Dimensions

CHAPTER 3
SOP PHYSICAL DIMENSIONS

3.1. SOP CASE OUTLINES

Intel's 32-lead TSOP meets the EIAJ and JEDEC registered standard.

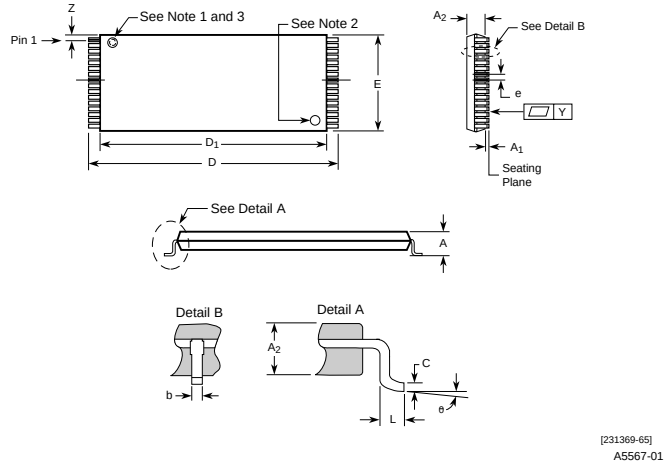


Figure 3-1. 32-Lead TSOP Package Drawing and Specifications

		Millimeters				Inches			
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A_1	0.050				0.002			
Package Body Thickness	A_2	0.965	0.995	1.025		0.038	0.039	0.040	
Lead Width	b	0.150	0.200	0.300		0.006	0.008	0.012	
Lead Thickness	c	0.100	0.150	0.200		0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	4
Package Body Width	E	7.800	8.000	8.200	4	0.307	0.315	0.323	4
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.000	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		32				32		
Lead Tip Angle	Ø	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

Intel's 40-lead TSOP meets the EIAJ and JEDEC registered standard.

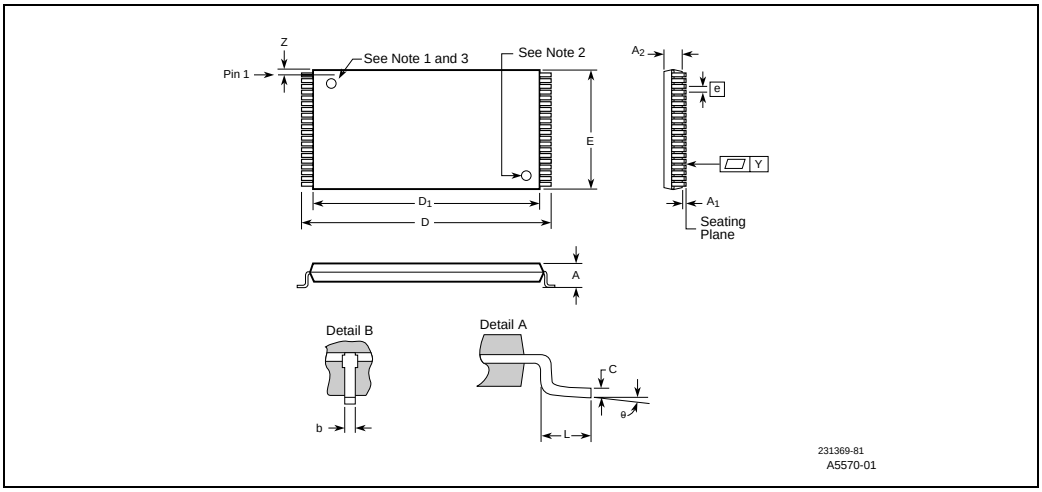


Figure 3-2. 40-Lead TSOP Package Drawing and Specifications

		Millimeters				Inches			
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A_1	0.050				0.002			
Package Body Thickness	A_2	0.965	0.995	1.025		0.038	0.039	0.040	
Lead Width	b	0.150	0.200	0.300		0.006	0.008	0.012	
Lead Thickness	c	0.100	0.150	0.200		0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	4
Package Body Width	E	9.800	10.000	10.200	4	0.386	0.394	0.402	4
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.00	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		40				40		
Lead Tip Angle	Ø	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

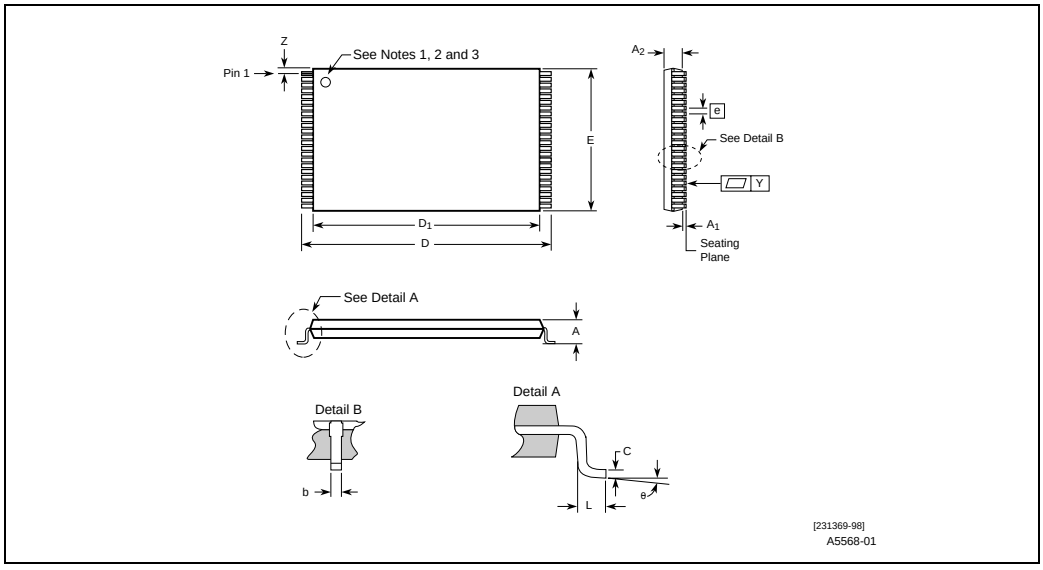
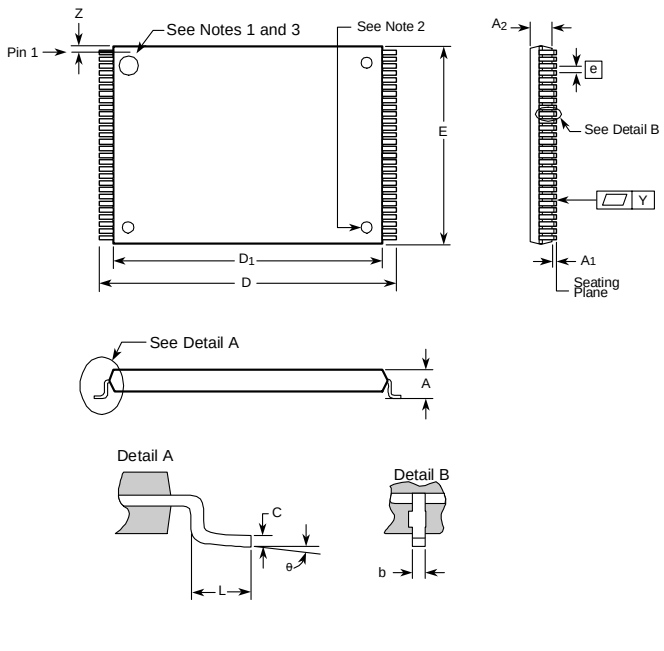


Figure 3-3. 48-Lead TSOP Package Drawing and Specifications

		Millimeters				Inches			
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A_1	0.050				0.002			
Package Body Thickness	A_2	0.950	1.000	1.050		0.037	0.039	0.041	
Lead Width	b	0.150	0.200	0.300		0.006	0.008	0.012	
Lead Thickness	c	0.100	0.150	0.200		0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	4
Package Body Width	E	11.800	12.000	12.200	4	0.465	0.472	0.480	4
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.000	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		48				48		
Lead Tip Angle	Ø	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

The 56-Lead TSOP meets the JEDEC registered standard. The same standard is being circulated for approval by EIAJ.



	Sym	Millimeters				Inches			
		Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A			1.200				0.047	
Standoff	A_1	0.050				0.002			
Package Body Thickness	A_2	0.965	0.995	1.025		0.038	0.039	0.040	
Lead Width	b	0.100	0.150	0.200		0.004	0.006	0.008	
Lead Thicknes	c	0.100	0.150	0.200		0.004	0.006	0.008	
Package Body Length	D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	4
Package Body Width	E	13.800	14.000	14.200	4	0.543	0.551	0.559	4
Lead Pitch	e		0.500				0.0197		
Terminal Dimension	D	19.800	20.00	20.200		0.780	0.787	0.795	
Lead Tip Length	L	0.500	0.600	0.700		0.020	0.024	0.028	
Lead Count	N		56				56		
Lead Tip Angle	∅	0°	3°	5°		0°	3°	5°	
Seating Plane Coplanarity	Y			0.100				0.004	
Lead to Package Offset	Z	0.150	0.250	0.350		0.006	0.010	0.014	

Figure 3-4. 56-Lead TSOP Package Drawing and Specifications

Thin Small Outline Package (TSOP)

Table 3-1. Symbol List for Thin Small Outline Package Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Standoff
A_2	Package Body Thickness
A_3	Lead Height
b	Width of Terminal Leads
c	Thickness of Terminal Leads
D_1	Plastic Body Length
E	Package Body Width
e	Lead Pitch
D	Terminal Dimension
L	Lead Foot Length
N	Total Number of Potentially Usable Lead Positions
Y	Seating Plane Coplanarity
Z	Lead to Package Offset
Ø	Lead Tip Angle

Packaging Family Attributes	
Category	Thin Small Outline Package
Acronym	TSOP
Lead Configuration	Dual-In-Line, Type I
Lead Counts	32, 40, 48, 56
Lead Finish	Solder Plate
Lead Pitch	0.5 mm
Board Assembly Type	Surface Mount

NOTES:

1-3. (1) If a dimple and a triangle are both present, the triangle denotes pin 1. (2) If only a dimple is present, it denotes pin 1. (3) If two dimples are present, the larger dimple denotes pin 1.

4. Profile Tolerance zones for D1 and E do not include mold protrusion. (Allowable mold protrusion on D1 is 0.25 mm per side and on E is 0.25 mm per side.

5. Lead Plating Thickness is 0.007 mm–0.015 mm. (Not part of b or c dimensions).

6. 32-, 40-, 48-, 56-Lead TSOP: Copper Alloy.

7. Novalac Body.

The 44-Lead PSOP meets the EIAJ registered standard. The same standard is being circulated for approval by JEDEC.

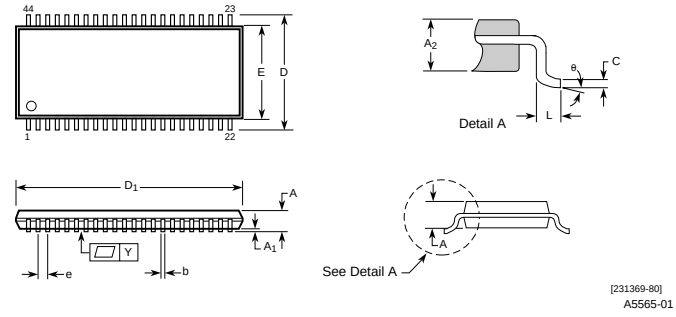
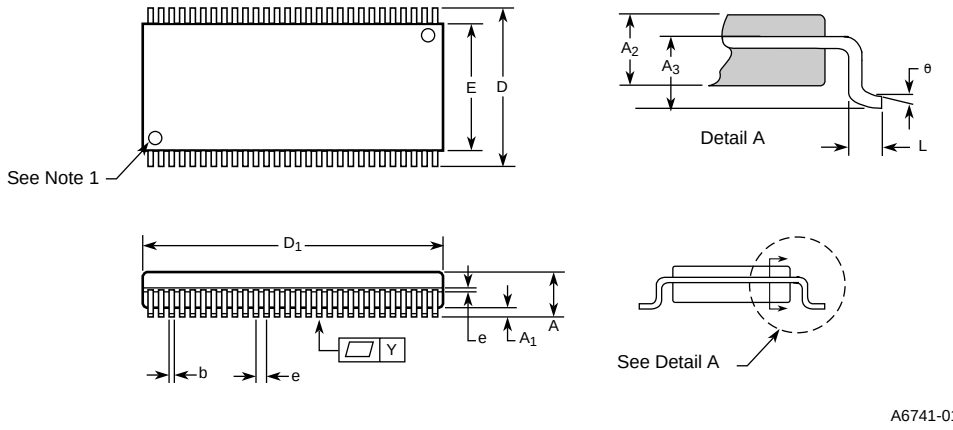


Figure 3-5. 44-Lead PSOP Package Drawing and Specifications

		Millimeters				Inches			
	Symbol	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**	**Notes**
Package Height	A			2.95				0.116	
Standoff	A_1	0.050				0.020			
Package Body Thickness	A_2	2.20	2.30	2.40		0.087	0.091	0.094	
Lead Width	b	0.35	0.40	0.50		0.014	0.016	0.020	
Lead Thickness	c	0.13	0.150	0.20		0.005	0.006	0.008	
Package Body Length	D_1	28.00	28.20	28.40	3	1.102	1.110	1.118	3
Package Body Width	E	13.10	13.30	13.50	3	0.516	0.524	0.531	3
Lead Pitch	e		1.27				0.050		
Terminal Dimension	D	15.75	16.00	16.25		0.620	0.630	0.640	
Lead Tip Length	L	0.75	0.80	0.85		0.030	0.031	0.33	
Seating Plane Coplanarity	Y			0.10				0.004	
Lead Tip Angle	Ø			8°				8°	



NOTE:

1. One dimple on package denotes Pin 1. If two dimples exist, Pin 1 will always be in the lower left corner of the package, in reference to the product mark.

Figure 3-6. 56-Lead SSOP Package Drawing and Specifications

		Millimeters				Inches			
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max	Notes
Package Height	A		1.80	1.90			0.070	0.075	
Standoff	A_1	0.47				0.018			
Package Body Thickness	A_2	1.18	1.28	1.38		0.046	0.050	0.054	
Lead Width	b	0.25	0.30	0.40		0.010	0.012	0.016	
Lead Thickness	c	0.13	0.15	0.20		0.005	0.006	0.008	
Package Body Length	D_1	23.40	23.70	24.00	3	0.921	0.933	0.945	3
Package Body Width	E	13.10	13.30	13.50	3	0.516	0.524	0.531	3
Lead Pitch	e		0.80				0.0315		
Terminal Dimension	D	15.70	16.000	16.30		0.618	0.630	0.642	
Lead Count	N		56				56		
Lead Tip Length	L	0.750	0.80	0.85		0.030	0.315	0.033	
Seating Plane Coplanarity	Y			0.10				0.004	
Lead Height	A_3	1.30	1.40	1.50		0.051	0.055	0.059	
Lead Tip Angle	Ø			5°				5°	

Plastic Small Outline Package/Shrink Small Outline Package (PSOP/SSOP)

Table 3-2. Symbol List for PSOP and SSOP Packages

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Standoff
A_2	Package Body Thickness
b	Width of Terminal Leads
c	Thickness of Terminal Leads
D_1	Plastic Body Length
E	Package Body Width
e	Lead Pitch
D	Terminal Dimension
L	Lead Tip Length
N	Total Number of Leads
Y	Seating Plane Coplanarity
Z	Lead to Package Offset
Ø	Lead Tip Angle

Packaging Family Attributes	
Category	Plastic Small Outline Package/Shrink Small Outline Package
Acronym	PSOP/SSOP
Lead Counts	44/56
Lead Finish	Solder Plate
Lead Pitch	1.27 mm/0.8 mm
Board Assembly Type	Surface Mount
Standard Registration	JEDEC and EIAJ

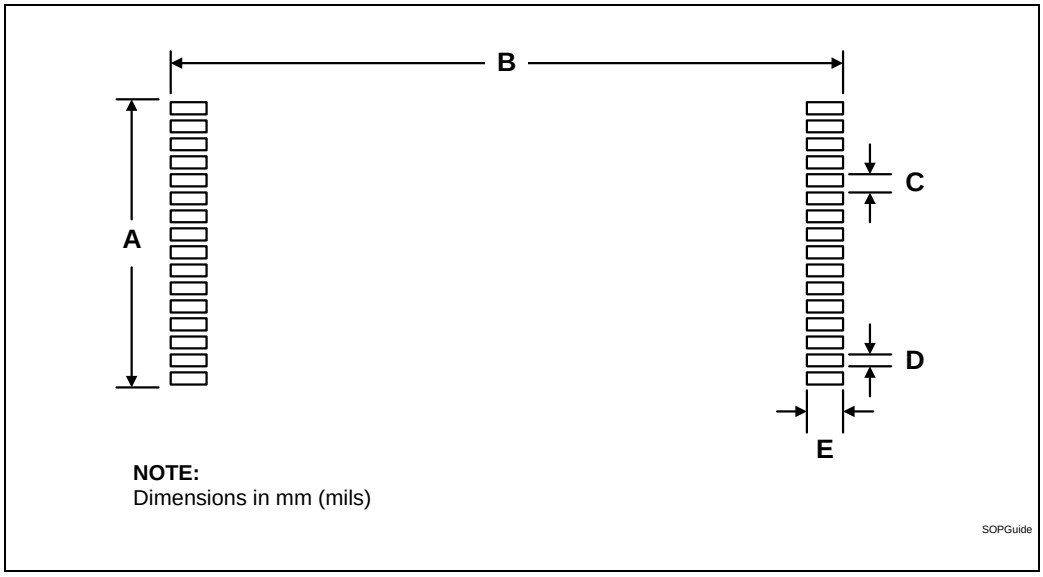
NOTES:

1. Copper Alloy 194.
2. Novalac Body.
3. Profile Tolerance zones for D1 and E do not include mold protrusion. (Allowable mold protrusion on D1 is 0.25 mm per side and on E is 0.15 mm per side.
4. Lead Plating Thickness is 0.007 mm–0.015 mm. (Not part of b or c dimensions).

3.2. SOP BOARD FOOTPRINTS

NOTE:

The WWW version of this document varies from the hard copy. Figures 3-7 through 3-9 have been deleted and replaced by the following figure and table in order to clarify the dimensions of typical TSOP, PSOP and SSOP land pads on line.



Typical Land Pad Diagram

Package Type	A	B	C	D	E
32-L TSOP	7.80 (307.1)	20.80 (818.9)	0.50 (19.7)	0.30 (11.8)	1.60 (63.0)
40-L TSOP	9.80 (385.8)	20.80 (818.9)	0.50 (19.7)	0.30 (11.8)	1.60 (63.0)
48-L TSOP	11.80 (464.6)	20.80 (818.9)	0.50 (19.7)	0.30 (11.8)	1.60 (63.0)
56-L TSOP	13.80 (543.3)	20.80 (818.9)	0.50 (19.7)	0.30 (11.8)	1.60 (63.0)
56-L SSOP	22.00 (866.1)	16.90 (665.4)	0.80 (31.5)	0.40 (15.7)	1.90 (74.8)
44-L PSOP	27.17 (1069.7)	16.90 (665.4)	1.27 (50.0)	0.50 (19.7)	1.90 (74.8)

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3.3. SOP COMPONENT VOLUME AND WEIGHT

Table 3.3 shows the component volume and weight of the SOP family.

Table 3-3. SOP Component Weight and Volume

Package	Max Height	Max Volume	Average Weight
32-Lead TSOP	1.20 mm	194.2 mm^3	0.37 gms
40-Lead TSOP	1.20 mm	247.2 mm^3	0.46 gms
48-Lead TSOP	1.20 mm	242.2 mm^3	0.56 gms
56-Lead TSOP	1.20 mm	344.2 mm^3	0.63 gms
44-Lead PSOP	2.95 mm	1,225.7 mm^3	1.89 gms
56-Lead SSOP	1.90 mm	681.1 mm^3	1.15 gms

4

SOP Package Characteristics

CHAPTER 4
SOP PACKAGE CHARACTERISTICS

4.1. SOP ELECTRICAL DATA

The electrical characteristics for Intel's SOP packages follow. The three parameters discussed are D.C. resistance (R), capacitance (C), and inductance (L). These characteristics vary slightly between each product contained in each package. Table 4-1 through Table 4-4 list the typical values for each package type and for each product in each package.

Table 4-1. 32-Lead TSOP Electrical Characteristics

Device	L (nH)	Pin C (pF)	Lead-to-Lead C (pF)
28F010	6.86–7.84	8–12	0.80–0.94
28F001BX	6.86–7.84	8–12	0.80–0.94
28F020	5.05–5.95	8–12	0.59–0.73

Table 4-2. 40-Lead TSOP Electrical Characteristics

Device	L (nH)	Pin C (pF)	Lead-to-Lead C (pF)
28F008SA	3.62–4.28	8–12	0.38–0.40
28F004BX	3.55–5.07	8–12	1.11–1.33
28F002BX	5.16–6.55	8–12	1.42–1.73

Table 4-3. 56-Lead TSOP Electrical Characteristics

Device	L (nH)	Pin C (pF)	Lead-to-Lead C (pF)
28F400BX	3.62–4.28	8–12	0.61–0.87
28F200BX	7.73–8.92	8–12	0.75–0.82
28F016	4.44–5.39	8–12	0.45–0.50

Table 4-4. 44 Cu L/F Lead PSOP Electrical Characteristics

Device	L (nH)	Pin C (pF)	Lead-to-Lead C (pF)
28F008SA	6.57–11.05	8–12	2.09–3.32
28F400BX	5.66–13.37	8–12	1.85–3.89
28F200BX	4.07–9.02	8–12	1.33–2.77

4.2. SOP PACKAGE THERMAL DATA

The Theta JA (θ_{JA}) and Theta JC (θ_{JC}) of the SOP packages shown in Table 4-5 are based on simulation data. Test verification data will be available in the future.

Table 4-5. θ_{JA} and θ_{JC} by Package

Package	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32-Lead TSOP	98	35
40-Lead TSOP	77	24
48-Lead TSOP	73	10
56-Lead TSOP	76	10
56-Lead DDTSOP	76	10
44-Lead PSOP-Cu	60	20
56-Lead SSOP-Cu	60	20

5

SOP Manufacturing

CHAPTER 5
SOP MANUFACTURING

5.1. SOP ASSEMBLY PROCESS FLOW

All SOP packages undergo a similar assembly process flow. This flow is shown in Figure 5-1.

Figure 5-1. SOP Assembly Flow Chart

5.2. SOP PACKAGE MATERIALS AND METHODS

Table 5-1 shows the materials and methods used in the SOP packages. Table 5-2 shows the properties of the molding compound used in the SOP packages.

Table 5-1. SOP Package Materials/Methods

Package Element	32 TSOP	40, 48, 56 TSOP/PSOP/SSOP
Lead Frame	Alloy 42	Copper
Die Attach Adhesive	Silver-Filled Epoxy (TSOP/PSOP), Thermoplastic Film (SSOP)	
Bond Wire	Gold	
Bond Wire Diameter	1.3 mils	
Bonding Method	Thermosonic	
Mold Compound	Low Stress Epoxy Novolac	
Lead Finish	Tin/Lead Solder Plate (85/15)	

Table 5-2. SOP Molding Compound Properties

Property	Value	Unit	Condition
Specific Gravity	1.87	•	
T_g	165	°C	
CTE1	1.3	$\times 10^{-5}$/°C	
CTE2	5.9	$\times 10^{-5}$/°C	
Volume Resistivity	1	$\times 10^{16}$ OHM cm	RT
	1	$\times 10^{13}$ OHM cm	150°C
Dielectric Constant	4.0	1 MHz	
Dissipation Factor	0.008	1 MHz	
Flammability	V–0	•	UL94

Table 5-3. EACEM Table

Substance	Weight (%)
Arsenic (As) M/C	trace 80 ppm of M/C
Barium (Ba)	—
Beryllium (Be)	—
Bromide (Br) M/C Bromated resin	0.7% of M/C
Cadmium (Cd)	—
Cobalt (Co)	—
Chromium (Cr)	—
Mercury (Hg)	—
Nickel (Ni) Leadframe A42 42% Ni	42% of LF (if A42)
Lead (Pb) Plating	15% of Plating
Antimony (Sb) M/C Antimony Oxide 2.5%	1.6% of M/C
Selenium (Se)	—
Tin (Sn) Plating	85% of Plating
Polybromide-biphenyl (PBB)	—
Polybromide-dipnenyloxide	—
Ozone-depleting substances	—

Figure 5-2 and Figure 5-3 show cross sections of the SOP packages. The figures show the nominal dimensions (in mm) of important internal package characteristics.

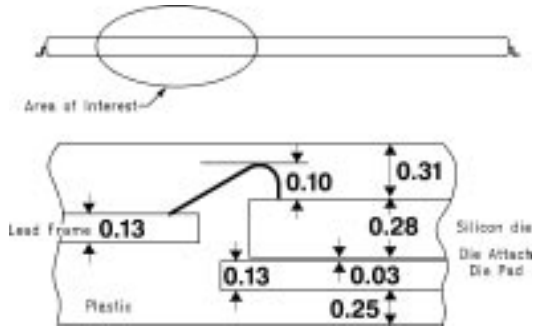

Figure 5-2. Typical TSOP Cross Section

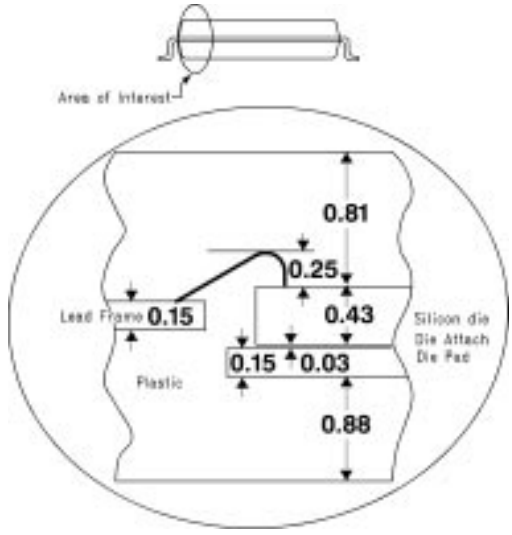

Figure 5-3. PSOP Cross Section

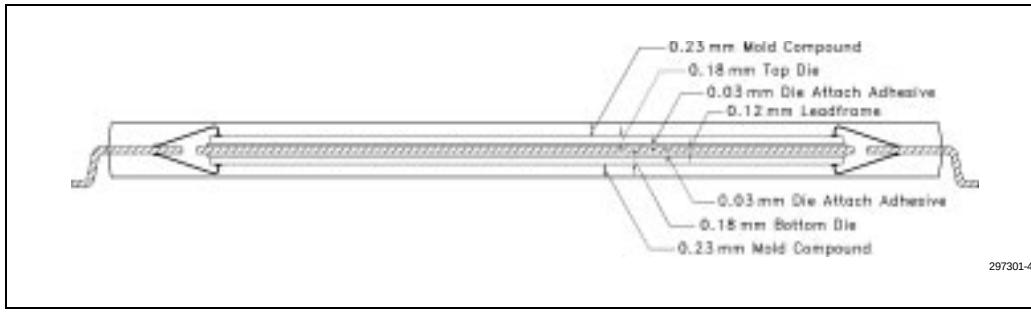

Figure 5-4. DDTSOP Cross Section

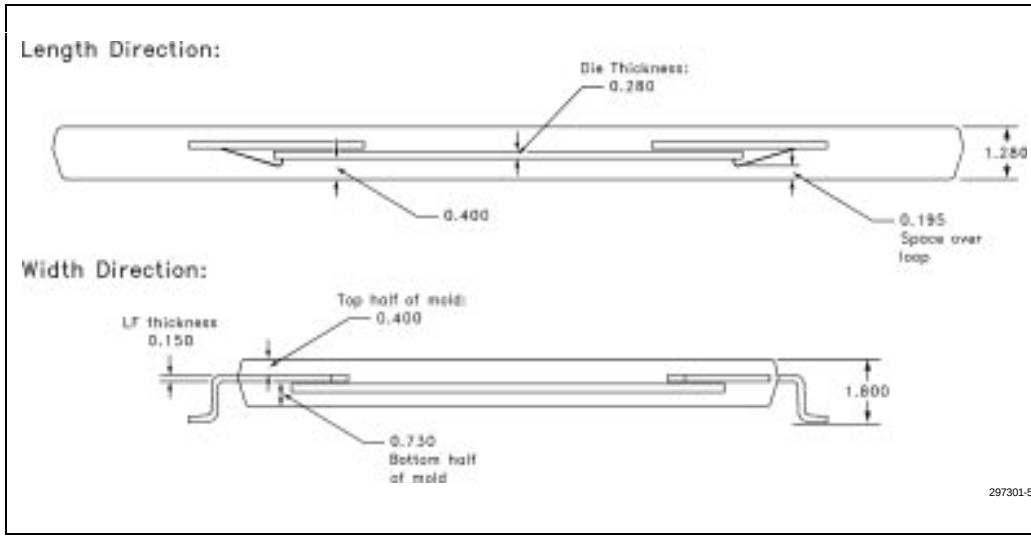

Figure 5-5. 56-L SSOP Cross Section

5.3. SOP TESTING

5.3.1. Electrical Test

Intel's 32-lead TSOP packages see an equivalent electrical test flow as Intel's 32-lead PLCC and PDIP products. This test flow ensures a level of electrical reliability consistent with that of our other packaged products.

Intel's new generation of flash memory devices are packaged in 40-lead TSOP, 48-Lead TSOP, 56-lead TSOP, 56-lead DDTSOP, 44-lead PSOP and 56-Lead SSOP. These devices see an optimized test flow that builds upon years of flash memory and EPROM production test experience. This test flow ensures the highest level of quality and electrical reliability.

Product handling of SOP products during test is done in a fully automated, tray to tray, pick and place fashion. This avoids any unnecessary contact with the leads, thus maintaining lead mechanical integrity.

Specific electrical tests vary slightly from product to product.

5.3.2. Solderability

The "area of interest" is defined as the bottom surface of the lead in the "gull" wing area. During the solderability test, a new coat of solder is added. Intel specifies a minimum of 90% coverage in the area of interest. The test consists of a two hour bake at 170°C, exposure to steam at one atmosphere of pressure for eight hours, fluxing in 25% R flux, and dipping in a solder pot at 219°C. The package is oriented so that the bottom of the lead enters the solder first.

5.3.3. Mechanical Inspection

100% of Intel's SOP products go through an outgoing inspection on an automated vision inspection system after test. This inspection ensures lead spacing, lead width, coplanarity, terminal dimension, foot length, and standoff all meet Intel's specifications. These specifications may be found in the *SOP Physical Dimensions*, Chapter 3.

6

SOP Reliability Stresses

CHAPTER 6
SOP RELIABILITY STRESSES

6.1. INTRODUCTION

The following information is written to provide users with the description and reliability summary of Intel's flash products in SOP packages. It includes brief test descriptions and the reliability data obtained during the qualification and subsequent product monitors.

6.2. TEMPERATURE CYCLING CONDITION "C"

Temperature cycling is performed to evaluate the mechanical integrity of the device when exposed to temperature extremes. Mechanical failure mechanisms such as package cracking, die cracking, thin film cracking, bond wire lifting, and die attach problems are accelerated by this stress. Temperature cycling also checks for changes in electrical characteristics due to mechanical displacement or rupture of conductors and insulating materials. Other effects can include delamination and degradation of package integrity. In this stress, the devices are alternately exposed to –65°C to +150°C (Condition C). The units must be transferred between temperatures within one minute. The units must be at that temperature for a minimum of ten minutes. The typical cycle time is approximately 26 minutes. Heating and cooling are done by convection. This test is conducted in conformance with specification Mil-Std-883C.

6.3. THERMAL SHOCK CONDITION "C"

Thermal shock is a liquid to liquid stress used to evaluate device resistance to sudden extreme changes in temperature. Thermal shock can result in die, package or thin film cracking, and delamination. Bond wire lifting and die attach problems are also accelerated by this stress. Thermal shock uses the same temperature ranges as temperature cycling, –65°C to +150°C (Condition C), but the units must be transferred between temperatures within ten seconds and are immersed in liquids at the specified temperature for five minutes. This test is conducted in conformance with specification Mil-Std-883C. Intel is in the process of phasing out this test for future products.

6.4. STEAM (AUTOCLAVE)

The steam stress accelerates moisture penetration through the plastic packaging material to the surface of the die. The objective of this test is to accelerate the problems found in very moist environments. Failure mechanisms typically seen from this stress include corrosion, passivation defects, leakage, and contamination. Passivation defects or marginalities can allow moisture penetration to a single flash cell causing oxide deterioration resulting in a charge loss failure. The test chamber is maintained at a temperature of 121°C and an absolute pressure of two atmospheres. The devices contain a 98%+ programmed pattern. After the stress the units are subjected to standard Intel testing. Units are mounted on interposers without bake prior to steam stressing, whenever necessary.

6.5. 85°C/85% RH

During the 85°C/85% relative humidity test, the devices are subjected to a high temperature, high humidity environment with alternate pins biased (+5V and ground). The object of the test is to accelerate failure mechanisms through an electrolytic process. This is accomplished through a combination of moisture penetration of the plastic, voltage potentials and contamination which, if present, would combine with the moisture to act as an electrolyte. Units are mounted on interposers without bake prior to testing, whenever necessary.

6.6. HIGH TEMPERATURE DYNAMIC LIFE TEST

This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. The parts are kept in the full active mode for the duration of the test with the outputs driven. A checkerboard data pattern is typically used to simulate random patterns expected during actual use. The test is intended to evaluate the long-term reliability of the product.

32-Lead TSOP

The 28F010, 28F001BX and 28F020 products are packaged in the 32-lead TSOP package. The data for the 28F010 and 28F020 is presented here, and may be extrapolated to the 28F001BX. All product was subjected to 85°C/85% RH preconditioning prior to stress.

Table 6-1. 28F010 32-Lead TSOP Reliability Data

28F010	Temperature Cycling				Thermal Shock			
Lot #	**200 Cyc**	**500 Cyc**	**1K Cyc**	**2K Cyc**	**50 Cyc**	**200 Cyc**	**500 Cyc**	**1K Cyc**
E Qual Lot 1	0/78	0/76	0/76	0/76	0/78	0/78	0/78	0/78
E Qual Lot 2	0/78	0/78	0/78	1/78	0/78	0/78	0/78	0/78
F Qual Lot 1	0/78	0/78	0/78	0/78	0/78	0/78	0/78	0/78
Total	0/234	0/232	0/232	1/232	0/234	0/234	0/234	0/234
				A				

28F010	Steam				85°C/85% RH			
Lot #	**24 Hrs**	**96 Hrs**	**168 Hrs**	**336 Hrs**	**168 Hrs**	**500 Hrs**	**1K Hrs**	**2K Hrs**
E Qual Lot 1	0/129	0/129	0/129	0/129	0/129	1/129	0/127	0/127
E Qual Lot 2	0/129	0/129	0/129	0/129	1/129	0/128	0/128	0/128
F Qual Lot 1	0/129	0/129	0/128	0/128	0/127	0/127	0/127	0/127
Total	0/387	0/387	0/386	0/386	1/385	1/384	0/382	0/382
					B	**C**		

NOTE:

All packages for steam and 85°C/85% RH were surface mounted (without bake) on 60mil FR4 interposers prior to stress.

28F010	Extended Life Test			
Lot #	**336 Hrs**	**500 Hrs**	**1K Hrs**	**2K Hrs**
E Qual Lot 1	0/92	0/92	0/92	0/92
E Qual Lot 2	0/96	0/96	0/96	0/96
F Qual Lot 1	0/96	0/96	0/94	0/0
Total	0/284	0/284	0/282	0/188

FAILURE SUMMARY:

A. 1 Power glitch—unit electrically overstressed during test

B. 1 Standby current failure, electrical overstress is suspected

C. 1 Standby current failure

Table 6-2. 28F020 32-Lead TSOP Reliability Data

28F020	Temperature Cycling				Thermal Shock			
Lot #	**200 Cyc**	**500 Cyc**	**1K Cyc**	**2K Cyc**	**50 Cyc**	**200 Cyc**	**500 Cyc**	**1K Cyc**
E Qual Lot 1	0/78	0/78	0/78	0/78	0/78	0/78	0/78	0/78
E Qual Lot 2	0/78	1/78	0/77	0/0	0/78	0/78	0/78	0/78
F Qual Lot 3	0/78	0/78	0/78	0/78	0/78	0/78	0/78	0/78
E Qual Lot 1	0/78	0/78	0/78	0/78	0/78	0/78	0/78	0/78
E Qual Lot 2	0/78	0/78	0/78	0/78	0/78	0/75	0/75	0/75
F Qual Lot 3	0/77	0/75	0/75	0/75	0/78	0/78	0/78	0/78
Total	0/467	1/465	0/464	0/387	0/468	0/465	0/465	0/465
		A						

28F020	Steam				85°C/85% RH		
Lot #	**24 Hrs**	**96 Hrs**	**168 Hrs**	**336 Hrs**	**168 Hrs**	**500 Hrs**	**1K Hrs**
E Qual Lot 1	0/129	0/129	0/129	0/129	0/129	0/129	0/129
E Qual Lot 2	0/129	0/129	0/129	1/129	1/129	0/128	0/128
F Qual Lot 3	0/129	0/129	0/129	0/129	0/129	0/129	0/129
E Qual Lot 1	0/129	0/129	0/129	0/129	1/127	0/126	0/126
E Qual Lot 2	0/129	0/129	0/129	0/129	0/126	0/126	0/126
F Qual Lot 3	0/129	0/129	0/129	0/129	0/129	0/129	0/129
Total	0/774	0/774	0/774	1/774	2/769	0/767	0/511
				B	**C**		

NOTE:

All packages for steam and 85°C/85% RH were surface mounted (without bake) on 60mil FR4 interposers prior to stress.

Table 6-2. 32-Lead TSOP Reliability Data (Continued)

28F020	Extended Life Test			
Lot #	**336 Hrs**	**500 Hrs**	**1K Hrs**	**2K Hrs**
E Qual Lot 1	0/96	0/96	0/96	0/96
E Qual Lot 2	0/96	0/96	0/96	0/0
F Qual Lot 3	0/96	0/96	0/96	0/0
E Qual Lot 1	0/96	0/96	0/96	0/96
E Qual Lot 2	0/96	0/96	0/95	0/95
F Qual Lot 3	0/96	0/96	0/94	0/94
Total	0/576	0/576	0/573	0/381

FAILURE SUMMARY:

A. 1 Basic function failure

B. 1 Charge loss, passivation defect found

C. 1 Standby current failure

1 Short

40-Lead TSOP

The 28F008SA, 28F002BX, and 28F004BX are packaged in a 40-lead TSOP package. The data for the 28F008SA may be extrapolated to the 28F002BX and 28F004BX. All product was preconditioned prior to stress using 85°C/85% RH preconditioning.

Table 6-3. 28F008SA 40-Lead TSOP Reliability Data

28F008SA	Temperature Cycling				Thermal Shock			
Lot #	**200 Cyc**	**500 Cyc**	**1K Cyc**	**2K Cyc**	**50 Cyc**	**200 Cyc**	**500 Cyc**	**1K Cyc**
E Qual Lot 4	0/80	0/80	0/80	0/80	0/80	0/80	0/80	0/80
E Qual Lot 5	0/80	0/79	0/79	0/79	0/80	0/80	0/80	0/80
F Qual Lot 1	0/44	0/44	0/44	0/44	0/45	0/45	0/45	0/45
F Qual Lot 2	0/45	0/45	0/45	0/45	0/45	0/45	0/45	0/45
Total	0/249	0/248	0/248	0/248	0/250	0/250	0/250	0/250

28F008SA	Steam				85°C/85% RH		
Lot #	**24 Hrs**	**96 Hrs**	**168 Hrs**	**336 Hrs**	**168 Hrs**	**500 Hrs**	**1K Hrs**
Qual Lot 1	0/80	0/80	0/80	0/80	0/55	0/55	0/55
Qual Lot 2	0/80	0/80	0/73	0/69	0/72	0/72	0/72
Qual Lot 3	0/81	0/81	0/76	0/68	0/125	0/125	0/125
Qual Lot 4	0/83	0/83	0/76	0/74	0/71	0/71	0/71
Qual Lot 5	0/45	0/45	0/45	0/44	0/70	0/70	0/70
Qual Lot 6	0/71	0/71	0/66	0/66	0/71	0/71	0/71
Qual Lot 7	0/74	0/74	0/74	1/73	0/72	0/72	—
Qual Lot 8	0/397	0/397	0/396	1/395	0/72	0/72	—
Total	0/911	0/911	0/886	0/869	0/608	0/608	0/464
				A		**B**	

NOTE:

All packages for steam and 85°C/85% RH were surface mounted (without bake) on 60mil FR4 interposers prior to stress.

Table 6.3 28F008SA 40-Lead TSOP Reliability Data (Continued)

28F008SA	Extended Life Test		
Lot #	**336 Hrs**	**500 Hrs**	**1K Hrs**
E Qual Lot 1	0/273	0/118	0/118
E Qual Lot 2	0/406	0/165	0/163
E Qual Lot 3	0/76	0/76	1/76
E Qual Lot 4	1/696	0/165	0/165
E Qual Lot 5	0/206	0/205	0/204
E Qual Lot 6	0/497	0/250	0/250
E Qual Lot 1	0/55	0/55	0/55
F Qual Lot 2	0/53	0/53	0/53
Total	1/2262	0/1087	1/1084
	C		**D**

FAILURE SUMMARY:

A. 1 V_{PP} current leakage failure
1 V_{PP} powerdown leakage

B. 2 Leakage failure

C. 1 Standby current failure

D. 1 Single bit charge loss

Table 6-4. 28F400CV 48-Lead TSOP Reliability Data

	Temperature Cycling				85°C/85% RH			Steam
Lot #	**500 Cycles**	**1K Cycles**	**1.5K Cycles**	**2K Cycles**	**168 Hrs**	**500 Hrs**	**1K Hrs**	**168 Hrs**
Qual Lot 1	0/85	0/85	1(A)/80	0/79	0/84	0/84	0/83	1(A)/85
Qual Lot 2	0/84	0/84	0/82	0/82	0/85	0/80	0/80	0/85
Qual Lot 3	0/85	0/85	0/83	0/83	0/85	0/81	0/81	0/85
Totals	0/254	0/254	1/245	0/244	0/254	0/245	0/244	1/255

FAILURE SUMMARY:

A. Lost Unit

56-Lead TSOP

The 28F200BX, 28F400BX and 28F016SA/SV are packaged in the 56-lead TSOP package.

Table 6-5. 28F200BX and 28F400BX 56-Lead TSOP Reliability Data

28F200BX	Temperature Cycling Condition "C"		
Lot #	**200 Cycles**	**500 Cycles**	**1000 Cycles**
Qual Lot 1	0/60	0/60	0/60
Qual Lot 2	0/60	0/60	0/60
Qual Lot 3	0/60	0/60	0/60
Total	0/180	0/180	0/180

28F200BX	85°C/85% RH		
Lot #	**168 Hours**	**500 Hours**	**1000 Hours**
Qual Lot 1	0/58	0/58	0/58
Qual Lot 2	0/60	0/60	0/60
Qual Lot 3	0/60	0/60	0/60
Total	0/178	0/178	0/178

28F200BX	Steam		
Lot #	**24 Hours**	**96 Hours**	**168 Hours**
Qual Lot 1	0/20	0/20	0/20
Qual Lot 2	0/20	0/20	0/20
Qual Lot 3	0/20	0/20	0/20
Total	0/60	0/60	0/60

Table 6.5 28F200BX and 28F400BX 56-Lead TSOP Reliability Data (Continued)

28F400BX	Temperature Cycling Condition "C"		
Lot #	**200 Cycles**	**500 Cycles**	**1000 Cycles**
Qual Lot 1	0/60	0/60	0/60
Qual Lot 2	0/60	0/60	0/60
Qual Lot 3	0/60	0/60	0/60
Total	0/180	0/180	0/180

28F400BX	85°C/85% RH		
Lot #	**168 Hours**	**500 Hours**	**1000 Hours**
Qual Lot 1	0/59	0/59	0/59
Qual Lot 2	0/60	0/60	0/60
Qual Lot 3	0/60	0/60	0/60
Total	0/179	0/179	0/179

28F400BX	Steam		
Lot #	**24 Hours**	**96 Hours**	**168 Hours**
Qual Lot 1	0/20	0/20	0/20
Qual Lot 2	0/20	0/20	0/20
Qual Lot 3	0/20	0/20	0/20
Total	0/60	0/60	0/60

Table 6-6. 28F016SA/SV 56-Lead TSOP Reliability Data

28F016SA	Temperature Cycling Condition "C"		
Lot #	**200 Cycles**	**500 Cycles**	**1000 Cycles**
Qual Lot 1	0/20	0/20	0/20
Qual Lot 2	0/20	0/19	0/19
Qual Lot 3	0/20	0/19	0/19
Total	0/60	0/59	0/59

28F016SA	Temperature Humidity Bias (85/85)		
Lot #	**168 Hours**	**500 Hours**	**1000 Hours**
Qual Lot 1	0/49	0/49	0/49
Qual Lot 2	0/61	0/61	0/61
Qual Lot 3	0/61	0/61	0/61
Qual Lot 4	0/61	0/61	0/61
Total	0/232	0/232	0/232

28F016SA	Steam	
Lot #	**48 Hours**	**168 Hours**
Qual Lot 1	0/38	0/38
Qual Lot 2	0/40	0/34
Qual Lot 3	0/40	0/40
Total	0/118	0/112

44-Lead PSOP

The 28F008SA, 28F400BX and the 28F200BX are packaged in the 44-lead PSOP package. The device used for this evaluation is a test chip designed for package certification and not production.

Table 6-7. 44-Lead PSOP Reliability Data

2XXXX	Temperature Cycling "C"					
Lot #	**1K Cyc**	**1.5K Cyc**	**2K Cyc**	**3K Cyc**	**4K Cyc**	**5K Cyc**
Qual Lot 1	1/40	0/39	0/39	0/39	0/39	0/39
Total	1/40	0/39	0/39	0/39	0/39	0/39
	A					

2XXXX	Temperature Cycling "B"					
Lot #	**1K Cyc**	**1.5K Cyc**	**2K Cyc**	**3K Cyc**	**4K Cyc**	**5K Cyc**
Qual Lot 1	0/40	0/40	0/40	0/40	0/40	0/40
Total	0/40	0/40	0/40	0/40	0/40	0/40

2XXXX	Steam				85°C/85% RH	
Lot #	**24 Hrs**	**96 Hrs**	**168 Hrs**	**336 Hrs**	**1K Hrs**	**2K Hrs**
Qual Lot 1	0/119	0/119	0/119	1/119	0/76	0/76
Total	0/119	0/119	0/119	1/119	0/76	0/76
				B		

NOTE:

All packages for steam and 85°C/85% RH were surface mounted (without bake) on 60mil FR4 interposers prior to stress.

FAILURE SUMMARY:

A. 1 Single bit charge loss due to passivation damage

B. 1 Single bit charge loss

56-Lead SSOP

The 28F016SA/SV is also packaged in the hi-rel 56-lead SSOP Package

Table 6-8. 28F016A/SV 56-Lead SSOP Reliability Data

DA28F016SA	Temperature Cycling Condition "C"		
Lot #	**500 Cycles**	**1000 Cycles**	**2000 Cycles**
Qual Lot 1	0/30	0/30	0/30
Qual Lot 2	0/30	0/30	0/30
Qual Lot 3	0/29	0/29	0/27
Qual Lot 4	0/30	0/30	0/30
Qual Lot 5	0/30	0/30	0/30
Total	0/149	0/149	0/147

DT28F016SA	Thermal Shock Condition "C"
Device	**200 Cycles**
Qual Lot 1	0/20
Qual Lot 2	0/131
Qual Lot 3	0/20
Qual Lot 4	0/10
Qual Lot 5	0/12
Total	0/75

DA28F016SA	Steam	
Lot #	**168 Hours**	**336 Hours**
Qual Lot 1	1/28A	0/26
Qual Lot 2	0/30	0/30
Qual Lot 3	0/29	0/29
Qual Lot 4	0/28	0/28
Qual Lot 5	0/28	0/28
Qual Lot 6	0/30	0/30
Total	01/174	1/163

Table 6-8. 28F016A/SV 56-Lead SSOP Reliability Data (Continued)

DA28F016SA	Temperature Humidity Bias (85/85)	
Lot #	**168 Hours**	**500 Hours**
Qual Lot 1	0/55	0/54
Qual Lot 2	0/54	0/53
Qual Lot 3	0/55	0/54
Qual Lot 4	0/54	0/54
Qual Lot 5	0/55	0/55
Qual Lot 4	0/55	
Total	0/328	0/270

Failure Analysis Summary

ID	Qty	Description
A	1	Under Analysis. No metal corrosion is visible.
B	1	Under Analysis

6.7. TSOP/PSOP SOLDER JOINT RELIABILITY

Background

TSOP or Thin Small Outline Packages have gained wide spread market acceptance throughout the electronics industry. This innovative extremely thin and small footprint package was designed to fill a need created by the form factor specified for use in PCMCIA[1] standard memory cards. The TSOP package/product system is one of the most robust systems in the marketplace. Leadframe material, leadframe design, plastic molding compound, and die design features were all integrally matched to provide a moisture insensitive package for the convenience of the customer.

However, with the broad and rapidly escalating acceptance of flash products in the marketplace, this small outline package is being considered for a multitude of other use conditions. While the package/product system is very robust, the small form factor and accordingly short stiff lead form construction could limit its application in certain situations. Specifically, applications requiring 20+ year lifetime or others using thick multi-layer FR4 PCBs may be at risk when the system is subject to extreme thermal cycling.

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[1] PCMCIA is the Personal Computer Memory Card Industry Association.

6.7.1. SMT Considerations

Solder joint reliability is predominantly determined by two separate factors. The first factor is the surface mount process itself. Without a good initial solder joint, you cannot expect good solder joint reliability. This fine pitch package (.5 mm/19.7 mil) requires different considerations than the more traditional 50 mil pitch type components. IR reflow profiles, solder volumes, and land pad layouts all contribute to the proper fillet formation and a defect free solder joint. Remember, you must start with a good SMT process to have reliable solder joints. The second factor is the use condition itself. Package/board configuration, operating conditions and thermal cycling of the board drive solder joint reliability. In order to determine if TSOP is the correct package for your application, various graphical presentations of failure rate versus service life are included.

6.7.2. About the Data

Solder joint reliability modeling was performed using various temperature cycle conditions. Data was taken using 64 mil thick FR4 boards of various layer count and 20 mil thick 4 layer memory cards. Temp cycle conditions A, B and C were performed and Weibull probability plots were developed for each condition. Acceleration factors for solder joint fatigue is given by Norris and Landsburg equations. These include frequency transformations, temperature swing transforms, and a factor for variation of ISO thermal fatigue characteristics of solder joints between test and operating conditions. These equations yield use condition graphs which are attached. The graphs provided show four different operational temperature swing conditions. Express, industrial, consumer, and computer conditions are depicted according to the IPC standards for these use variables. The extreme of the temperature swing and the frequency of swings per day modulate the solder joint reliability. We have included both temp cycle condition A and B test data and modeled projections based on those. We feel that condition A more directly simulates real life use condition. Condition B and C were used as highly accelerated conditions to obtain accelerated, but preliminary, failure predictions. As shown in temp cycle A cycling data, 50% failure point takes approximately six months to complete.

PSOP data has been included for completeness. PSOP and SSOP solder joint reliability is outstanding across applications and temperature ranges.

6.7.3. Conclusion

By using these graphs and the accompanying data, you can ascertain the expected failure rate for your particular use condition. With a good SMT process and the correct understanding of the use conditions, Intel Flash TSOP products are one of the most reliable product/package systems available in the marketplace today.

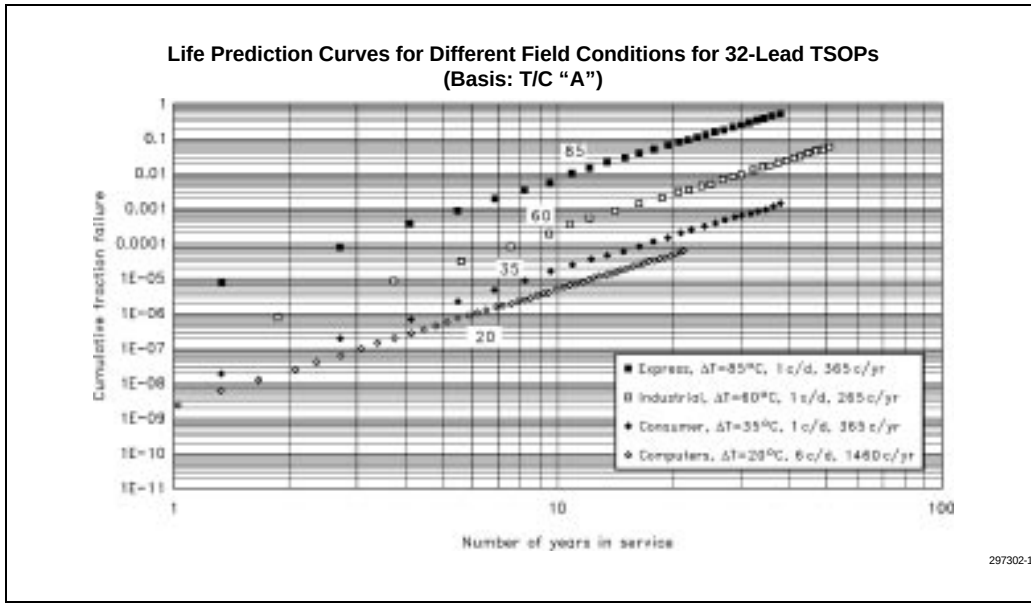


Figure 6-1. 32-Lead TSOP Life Prediction Curves

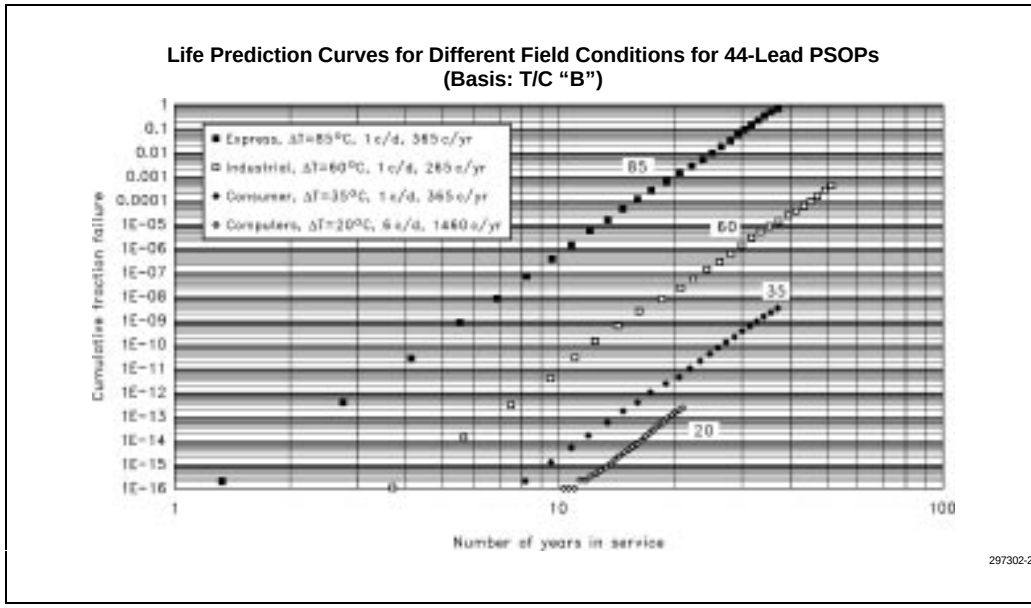


Figure 6-2. 44-Lead PSOP Life Prediction Curves

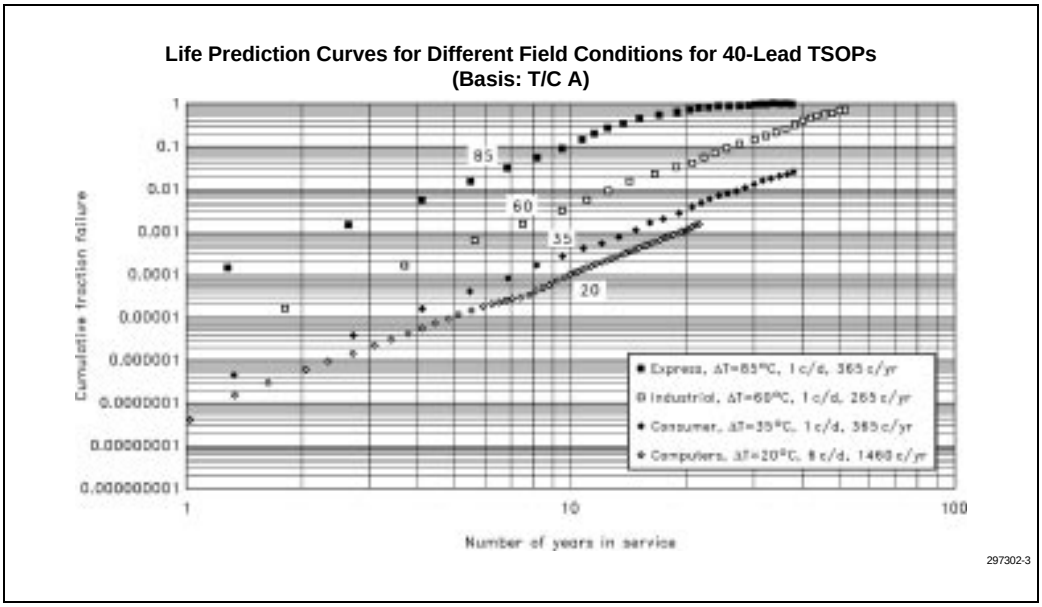


Figure 6-3. 40-Lead TSOP Life Prediction Curves

Table 6-9. 32-Lead TSOP Solder Joint Temp Cycle Results 60 MIL Thick FR-4 Boards (valid failures only)

T/C A (–55°C to +85°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K	4.5K	5.0K	5.5K	6.0K	6.5K	7.0K	7.5K	8.0K	8.5K	9.0K
Samples	22	22	22	22	22	22	22	22	22	22	22	22	22	22	20	17	17	15	15
Rejects	0	0	0	0	0	0	0	0	0	0	0	0	0	2	3	0	2	0	1
% CUM	0	0	0	0	0	0	0	0	0	0	0	0	0	9	23	23	32	32	36

22 Units X 32-Leads = 704 Solder Joints.

T/C B (–55°C to +125°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K
Samples	22	22	22	21	21	21	17	12	10
Rejects	0	0	1	0	0	4	5	2	4
% CUM	0	0	5	5	5	23	45	55	73

22 Units X 32-Leads = 704 Solder Joints.

T/C C (–65°C to +150°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K
Samples	22	22	22	21	20	17	15	10	4
Rejects	0	0	1	1	3	2	5	6	1
% CUM	0	0	5	9	23	32	55	82	86

22 Units X 32-Leads = 704 Solder Joints.

Table 6-10. 32-Lead TSOP Mounted On 20 MIL/4 Layer FR-4 Memory Cards

T/C A (–55°C to +85°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K	4.5K	5.0K	5.5K	6.0K	6.5K	7.0K	7.5K	8.0K	8.5K	9.0K
Samples	66	66	66	66	66	66	66	66	66	44	44	44	44	44	44	44	44	44	44
Rejects	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
% CUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

66 Cards X 8 TSOPS/Memory Card X 32 Joints/TSOP = 16,896 Joints.
Sample Size Reduced At 4.5K Hour Readout.

Table 6-11. 40-Lead TSOP Solder Joint Temp Cycle Results 60 MIL Thick FR-4 Boards (valid failures only)

T/C A (–55°C to +85°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K	4.5K	5.0K	5.5K	6.0K	6.5K
Samples	32	32	32	32	32	31	30	30	30	26	24	22	16	10
Rejects	0	0	0	0	1	1	0	0	4	2	2	6	6	3
% CUM	0	0	0	0	3	6	6	6	19	25	31	50	69	78

32 Units X 40-Leads = 1280 Solder Joints.

T/C B (–55°C to +125°C)

Cycles	200	500	1.0K	1.5K	2.0K	2.5K	3.0K
Samples	32	32	31	26	12	4	1
Rejects	0	1	5	14	8	3	1
% CUM	0	3	19	63	88	97	100

32 Units X 40-Leads = 1280 Solder Joints.

Table 6-12. 44-Lead PSOP Solder Joint Temp Cycle Results 60 MIL Thick FR-4 Boards (valid failures only)

T/C A (–55°C to +85°C)

Cycles	1.0K	2.0K	3.0K	4.0K	5.0K	6.0K	7.0K	8.0K	9.0K	10K	11K	12K	13K
Samples	22	22	22	22	22	22	22	22	22	22	22	22	22
Rejects	0	0	0	0	0	0	0	0	0	0	0	0	0
% CUM	0	0	0	0	0	0	0	0	0	0	0	0	0

22 Units X 44-Leads = 968 Solder Joints.

T/C B (–55°C to +125°C)

Cycles	500	1.0K	1.5K	2.0K	2.5K	3.0K	3.5K	4.0K	4.5K	5.0K	5.5K	6.0K	6.5K
Samples	22	22	22	22	22	22	22	22	22	22	22	20	18
Rejects	0	0	0	0	0	0	0	0	0	0	2	2	7
% CUM	0	0	0	0	0	0	0	0	0	0	9	18	50

22 Units X 44-Leads = 968 Solder Joints.

7

SOP Handling

CHAPTER 7
SOP HANDLING

7.1. SOP SHIPPING FORMATS/INFORMATION (TRAYS, TAPE, TUBES)

7.1.1. SOP Trays

Intel ships SOP product in JEDEC standard dimension trays. All JEDEC standard trays have the same outside dimensions and thus are stackable for ease of storage and manufacturing. The device leads are kept from touching any part of the tray by design. SOP thick tray physical dimensions are illustrated in Figures 7-1 and 7-2 and are detailed in Table 7.1. SOP thin tray physical dimensions are illustrated in Figures 7-3 and 7-4 and are detailed in Table 7.2.

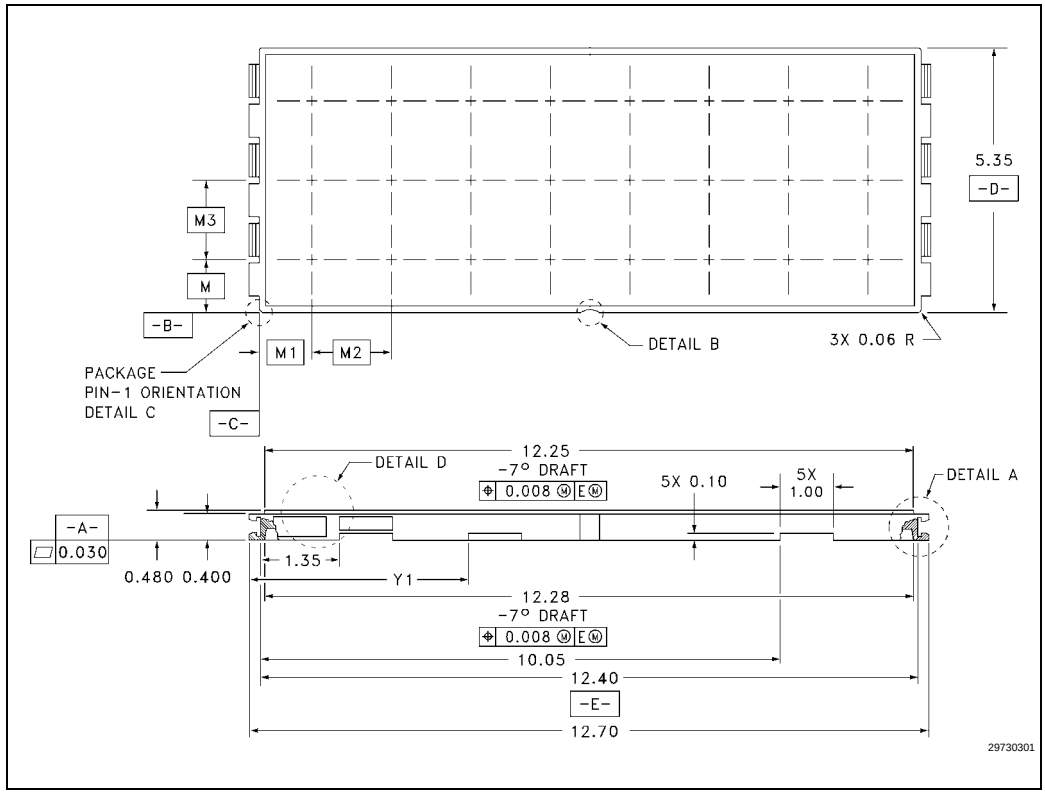


Figure 7-1. SOP Thick Tray Diagram

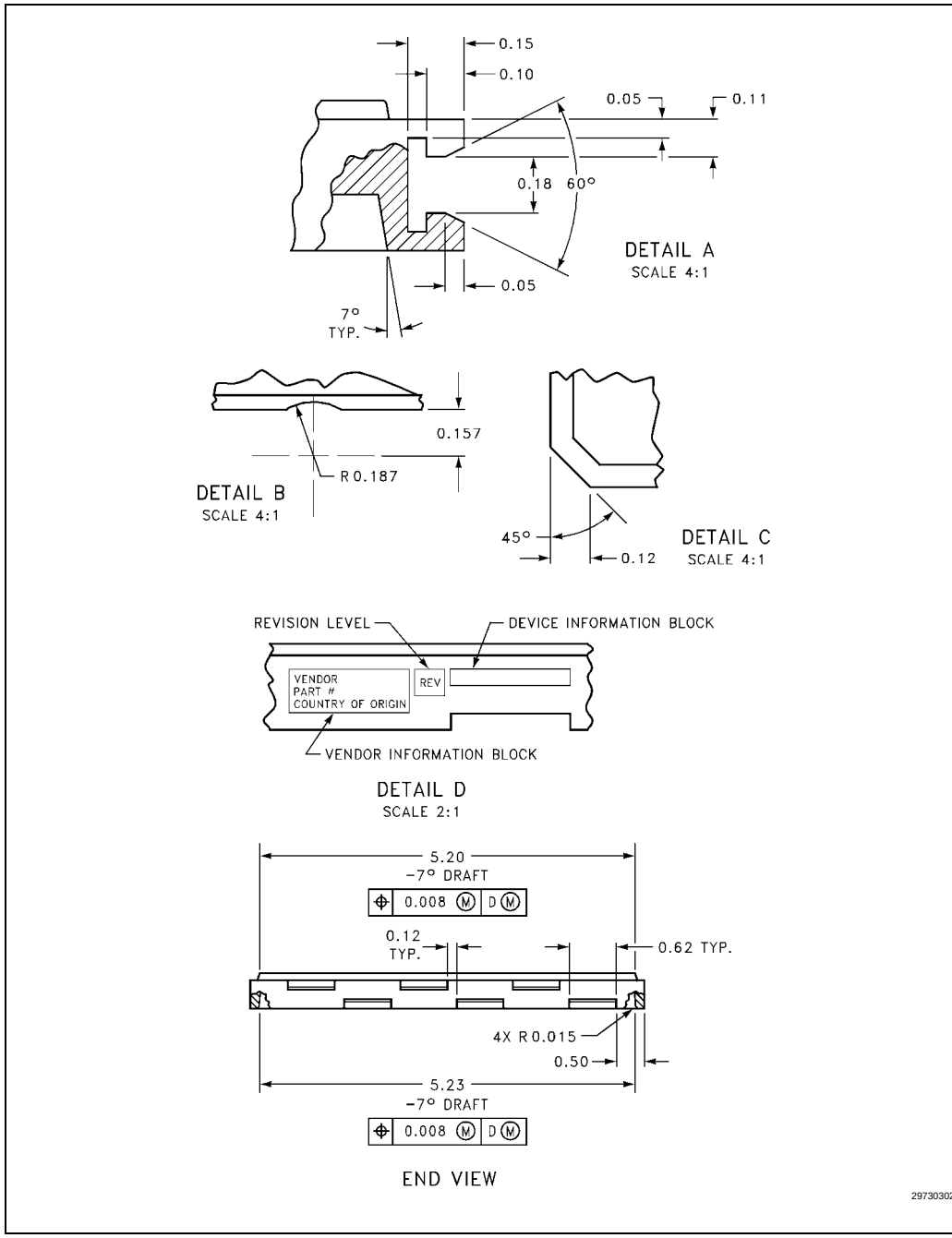


Figure 7-2. SOP Thick Tray Diagram (Detailed View)

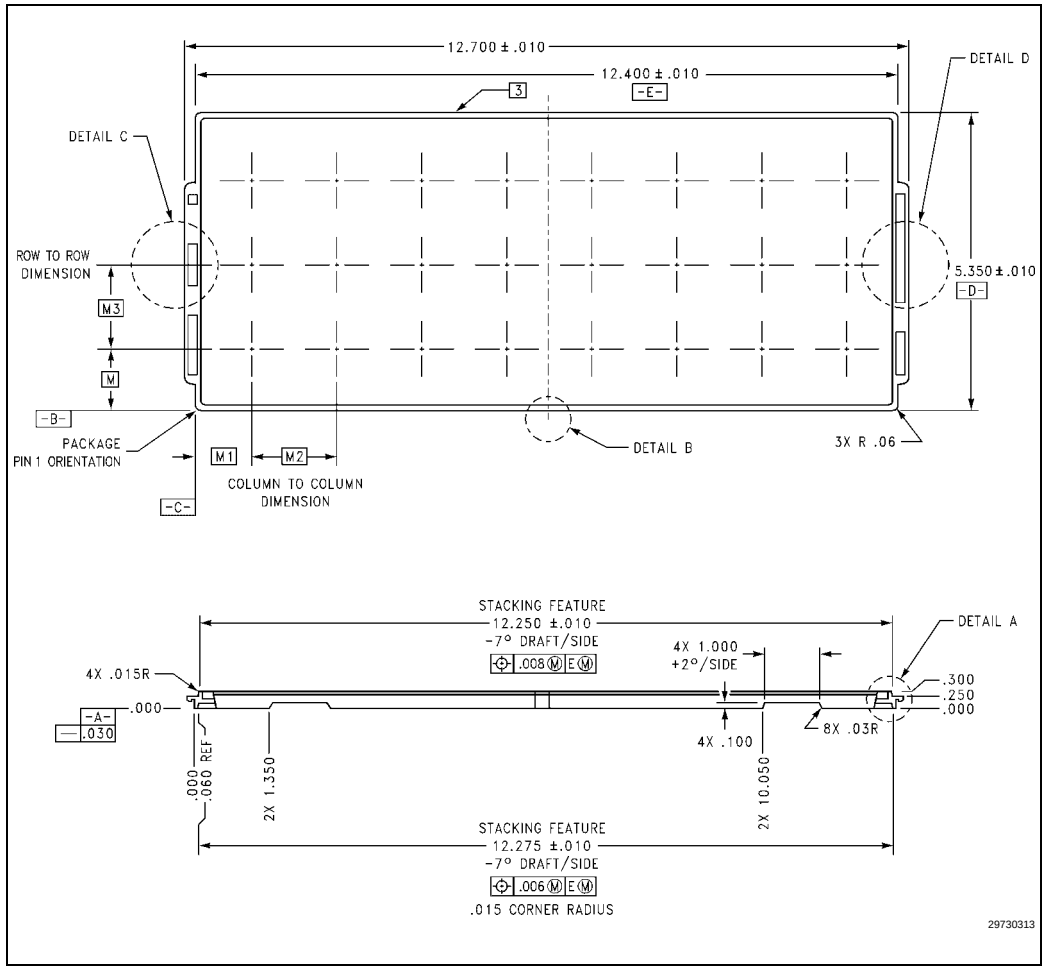


Figure 7-3. SOP Thin Tray Diagram

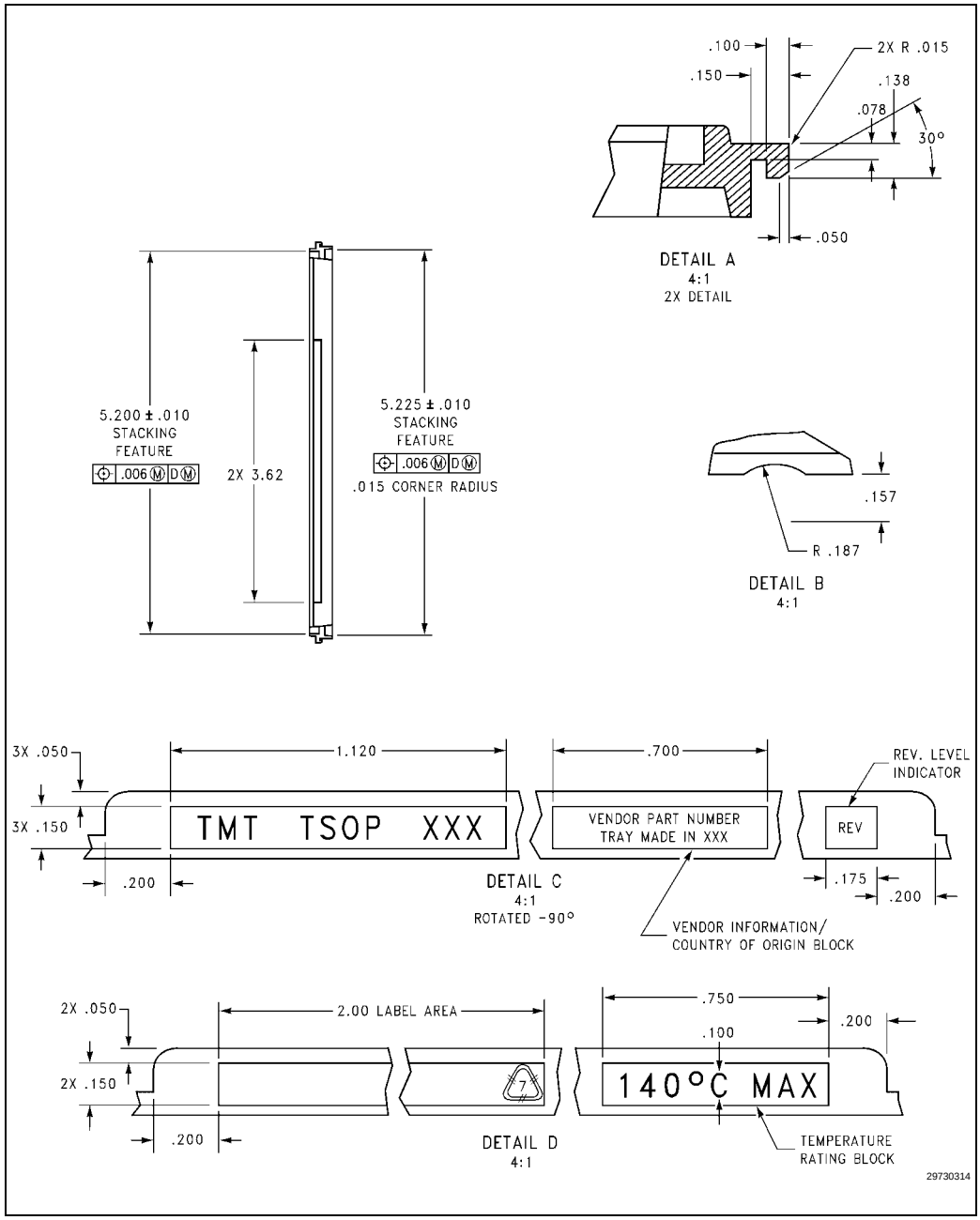


Figure 7-4. SOP Thin Tray Diagram (Detailed View)

Table 7-1. SOP Thick Tray Physical Dimensions

	32-Lead TSOP	40-Lead TSOP	48-Lead TSOP	56-Lead TSOP	56-Lead SSOP	44-Lead PSOP
Pocket Center Location to Edge Y (M)	10.24	18.49	17.27	17.27	13.61	20.85
Pocket Center Location to Edge X (M1)	29.46	29.46	29.46	29.46	29.46	31.78
Pocket Center Location to Center Distance X (M2)	32.00	32.00	32.00	32.00	32.00	35.92
Pocket Center Location to Center Distance X (M3)	16.48	16.48	16.89	16.89	18.11	23.55
# of Rows	8	7	7	7	7	5
# of Columns	9	9	9	9	9	9
Total # of Pockets	72	63	63	63	63	40

NOTE:
Dimensions in millimeters

Table 7-2. Thin High Density SOP Tray Dimensions

	32-Lead TSOP	40-Lead TSOP	48-Lead TSOP	56-Lead TSOP
Intel/3M Tray Part Numbers	21002-387-145	21002-386-145	21001-378-129	21002-385-145
Pocket Center Location to Edge Y (M)	8.53	14.40	15.80	13.00
Pocket Center Location to Edge X (M1)	17.25	17.25	17.25	17.24
Pocket Center Location to Center Distance X (M2)	25.50	25.50	25.50	25.50
Pocket Center Location to Center Distance X (M3)	9.90	11.898	14.90	15.69
# of Rows	13	10	8	8
# of Columns	12	12	12	12
Total # of Pockets	156	120	96	96

NOTE:
Dimensions in millimeters

7.1.2. Tray Recycling

Environmental Programs Overview

Intel continues to evaluate current packaging methodologies to ensure we meet or exceed global regulatory compliance with regards to environmental concerns. Our philosophy focuses on eliminating redundant or mixed materials as appropriate, implementation of reuse applications and increasing the recyclability of our component packaging material. For the latest information regarding reuse or recycling programs please contact 1-800-628-8686.

Tray Reuse Programs/Tray Suppliers

Intel has been very sucessful in establishing a program for reuse of our low/high temperature JEDEC Trays. Not only does the program offer a nominal cash reimbursement but it lowers the cost of plastic shipping trays, employs several handicapped agencies and reduces environmental waste. JEDEC trays can now be returned for reuse at Intel through a variety of methods dependent upon your location. To ensure trays are returned in a usable condition, trays should be placed in corrugated containers and palletized if volumes warrant. All containers should be labeled with the customer's return address.

North and South America Micro Plastics 3420 West Whitton Ave. Phoenix, AZ 85017 Phone: (602) 278-4545 Fax: (602) 278-4477	Contact Micro Plastics for specific Intel shipping instructions for your area. Bill Shipping Costs to: Intel Corp. C/O NWTA PO Box 4567 Federal Way, WA 98063
Asia Pacific Region Mr. Danny Tong Peak Plastic/SemiCycle Hong Kong LTD Unit 7, 37/F., Warf Cable Tower 9 Hoi Shing Road Tsuen Wan, NT, Hong Kong Phone: (852) 2402 5100 Fax: (852) 2498 5382	Peak Plastic will provide all shipping arrangements at no charge to the customer.
Japan Cygnus, Inc. 5-25-16, Naritahigashi Suginami-Ku, Tokyo, 166 Japan Phone: [81] 333-920370 Fax: [81] 333-920850	Contact Cygnus for shipping instructions.
Europe Peak Plastic/Semicycle PO Box 129 1211 Geneva 20 Switzerland Phone: 00 [41] 22-733-6282 Fax: 00 [41] 22-734-1479	Peak Plastic will provide all shipping arrangements at no charge to the customer

All trays will be subjected to a variety of inspections to ensure they meet Intel's specifications prior to reuse by an Intel factory. Any tray that fails Intel's quality requirements or non-Intel trays are sent to plastic reclamation vendors for utilization in other plastic applications. No trays are sent to landfills.

7.1.3. Tray Supplier/Brokers

Intel Flash SOP JEDEC trays are available from a number of tray recyclers and/or suppliers. The following list provides contact information for some suppliers.

Address	Phone
Micro Plastics **(Intel Primary source)** 3420 West Whitton Ave. Phoenix, AZ 85017	Telephone: (602) 278-4545 Fax: (602) 278-4477
EcoTech **(USA)** 3281 Keller Street Santa Clara, CA 95054	Telephone: (408) 988-2050 Fax: (408) 988-4009
Global Tech **(USA)**	Telephone: (408) 475-3588
Worltek Peak Plastics **(USA)** 2111 Kramer Lane Austin, TX 78758	Telephone: (800) 580-7364
Peak EEMS **(Europe)** Meikie Underhill West Kilbride KA23 9PE Scotland	Tel/Fax: (44) 1294 829856
Peak Plastics & Metal **(Asia Pacific Region)** Unit 4, 5, and 7, 37F Wharf Cable Tower 9 Hoi Shing Road Tsuen, N.T., Hong Kong	Telephone: (852) 2402-5100/2402-5101 Fax: (852) 2498-5382/2492-6563
3M Corporation **(New Intel Trays)** (250 Qty. Min. Order)	Telephone: 1 (800) 328-0411

7.1.4. SOP Tape and Reel

Intel's TSOP, SSOP and PSOP products are also offered in Tape and Reel format, suitable for automated SMT assembly equipment. The Tape and Reel packing system used on automated assembly equipment places the SOPs in a tape embossed with individual carrier packets. The devices are then sealed with a cover tape to retain them and for protection. The loaded tapes are next wound onto a reel similar to a movie reel. SOP Tape and Reel physical dimensions are illustrated in Figures 7-5, 7-6, and 7-7. and are described in Table 7.3, 7.4, and 7.5.

For Tape and Reel supplies, contact your local Advantek distributor or call Advantek at (612) 938-6800.

Please contact your local Intel representative for more information.

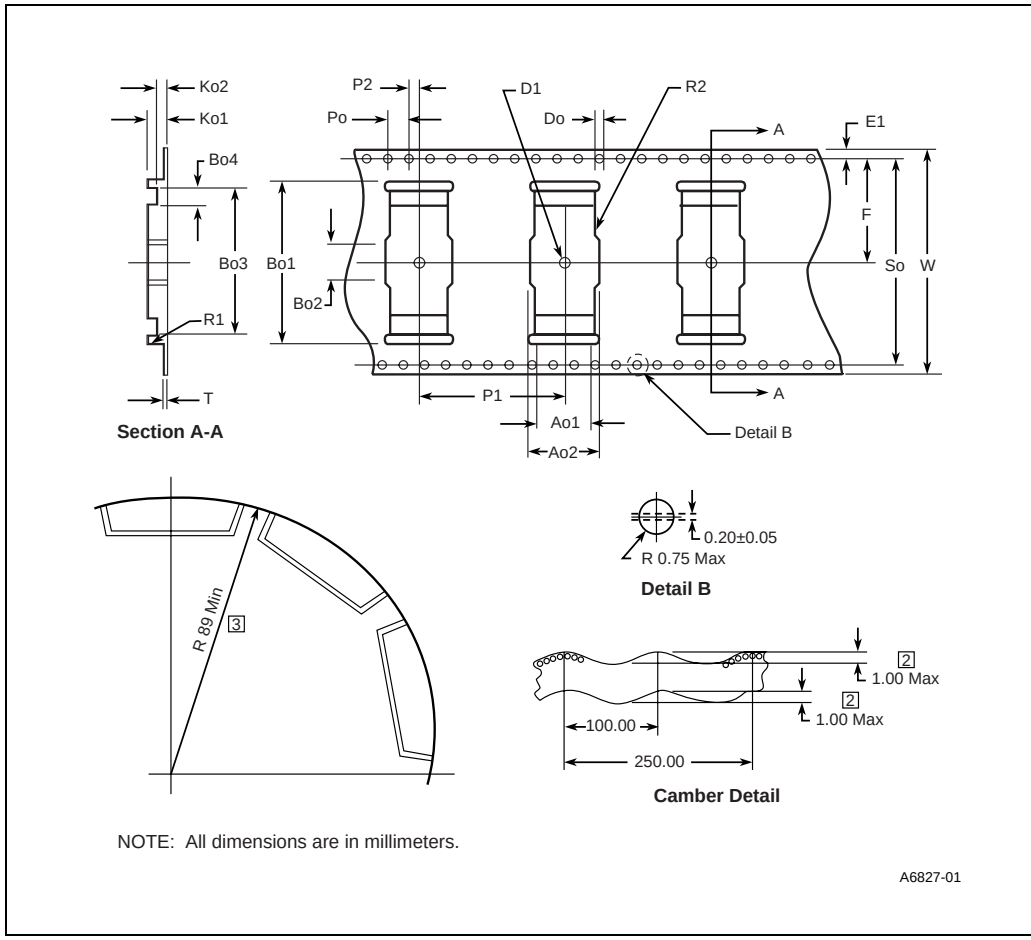
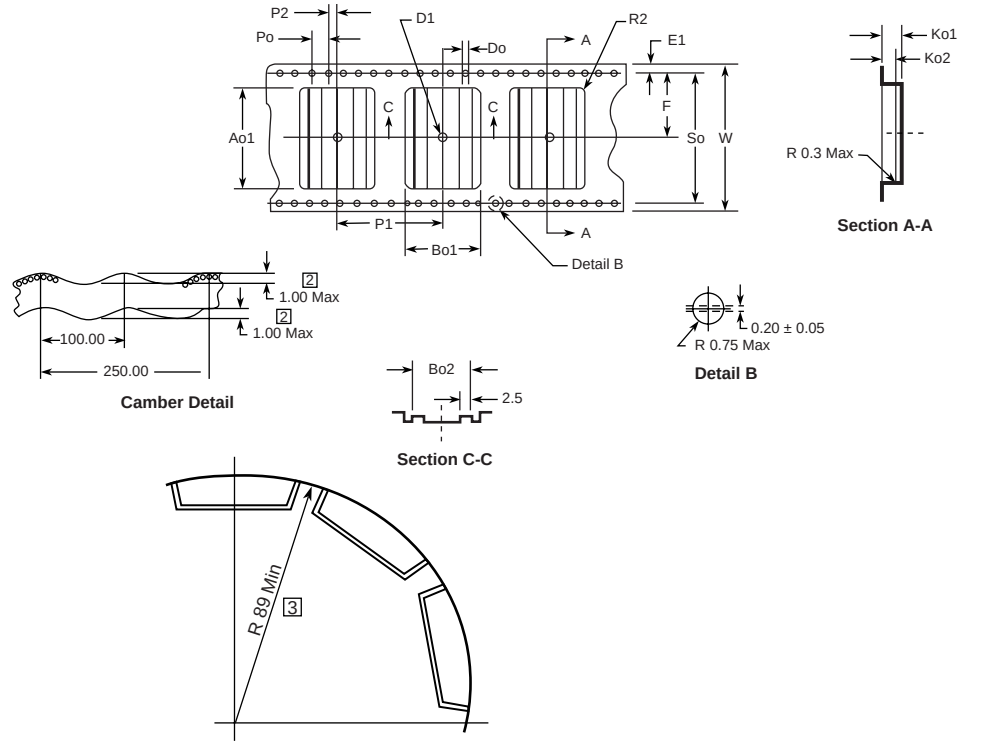


Figure 7-5. TSOP Tape and Reel Carrier Tape Diagram

Table 7-3. TSOP Carrier Tape Dimensions by Package

Symbol	Advantek Carrier Tape Part Numbers			
	TSOP32-BC90.OP2	**TSOP40-BC90.OP2**	**TSOP48-CC99.OP2**	**TSOP56-AC95.OP2**
Ao1	8.2–8.4	10.2–10.4	12.6–12.8	14.1–14.3
Ao2	9.9–10.1	11.9–12.1	13.9–14.1	16.0–16.2
Bo1	20.1–20.3	20.1–20.3	20.4–20.6	20.1–20.3
Bo2	3.9–4.1	3.9–4.1	3.9–4.1	3.9–4.1
Bo3	17.91–18.11	17.91–18.11	17.91–18.11	17.91–18.11
Bo4	2.4–2.6	2.4–2.6	2.4–2.6	2.4–2.6
Do	1.5–1.6	1.5–1.6	1.5–1.6	1.5–1.6
D1	1.95–3.0	1.95–3.0	1.95–3.0	1.95–3.0
E1	1.65–1.85	1.65–1.85	1.65–1.85	1.65–1.85
F	14.1–14.3	14.1–14.3	14.1–14.3	14.1–14.3
Ko1	1.6–1.8	1.6–1.8	1.6–1.8	1.6–1.8
Ko2	1.06–1.14	1.06–1.14	1.06–1.14	1.06–1.14
Po	3.9–4.1	3.9–4.1	3.9–4.1	3.9–4.1
P1	15.9–16.1	15.9–16.1	15.9–16.1	19.9–20.1
P2	1.9–2.1	1.9–2.1	1.9–2.1	1.9–2.1
R	50.0 Min	50.0 Min	50.0 Min	50.0 Min
R1	R 0.3 Max	R 0.3 Max	R 0.3 Max	R 0.3 Max
R2	R 0.5 Typ	R 0.5 Typ	R 0.5 Typ	R 0.5 Typ
So	28.3–28.5	28.3–28.5	28.3–28.5	28.3–28.5
T	0.25–0.35	0.25–0.35	0.25–0.35	0.25–0.35
W	31.7–32.3	31.7–32.3	31.7–32.3	31.7–32.3
Tape Size	**32 mm**	**32 mm**	**32 mm**	**32 mm**
Use for These Packages	**32-Lead TSOP**	**40-Lead TSOP**	**48-Lead TSOP**	**56-Lead TSOP**
Units/Reel	2000	2000	2000	1600



NOTE: All dimensions are in millimeters.

A6829-01

Figure 7-6. 44 mm, 44-Lead PSOP/56-Lead SSOP Tape and Reel Carrier Tape Diagram

Table 7-4. PSOP/SSOP Carrier Tape Dimensions by Package

Symbol	Advantek Carrier Tape Part Numbers	
	PSOP44-BC57.OP2	**SSOP56-DC83.OP2**
Ao1	28.6–28.8	24.2–24.4
Bo1	16.45–16.65	16.5–16.7
Bo2	13.05–13.25	12.4–12.6
Do	1.5–1.6	1.5–1.6
D1	2.0–3.0	2.0–3.0
E1	1.65–1.85	1.65–1.85
F	20.05–20.35	20.05–20.35
Ko1	3.37–3.57	2.3–2.5
Ko2	2.45–2.53	1.4–1.6
Po	3.9–4.1	3.9–4.1
P1	31.9–32.1	23.9–24.1
P2	1.85–2.15	1.85–2.15
R	89.0 Min	100.0 Min
R1	R 0.3 Max	R 0.3 Max
R2	R 0.5 Typ	R 0.5 Typ
So	40.3–40.5	40.3–40.5
T	0.25–0.35	0.25–0.35
W	43.7–44.3	43.7–44.3
Tape Size	**44 mm**	**44 mm**
Use for These Packages	**44-Lead PSOP**	**56-Lead SSOP**
Units/Reel	450	700

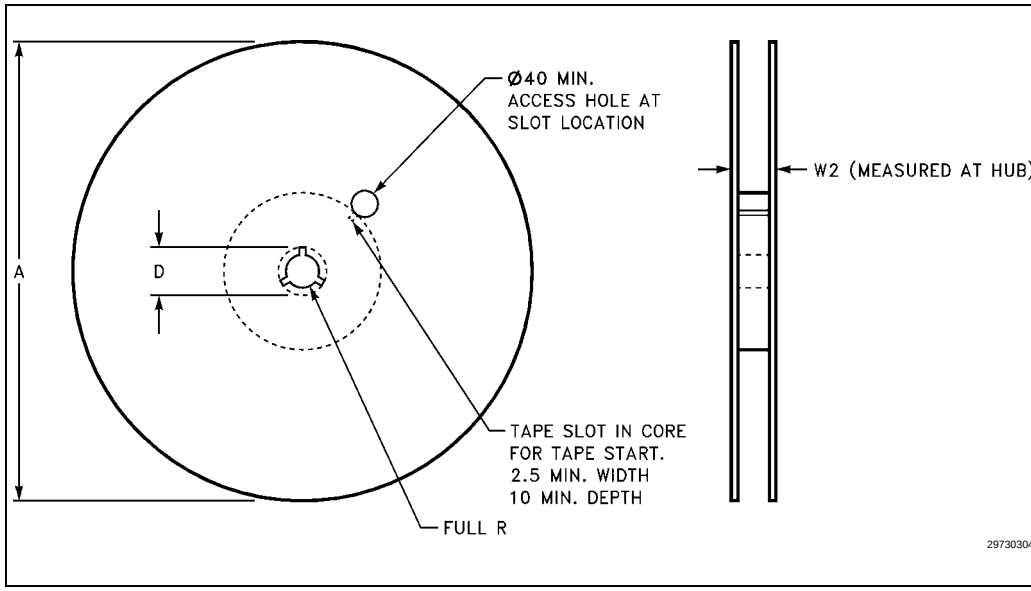
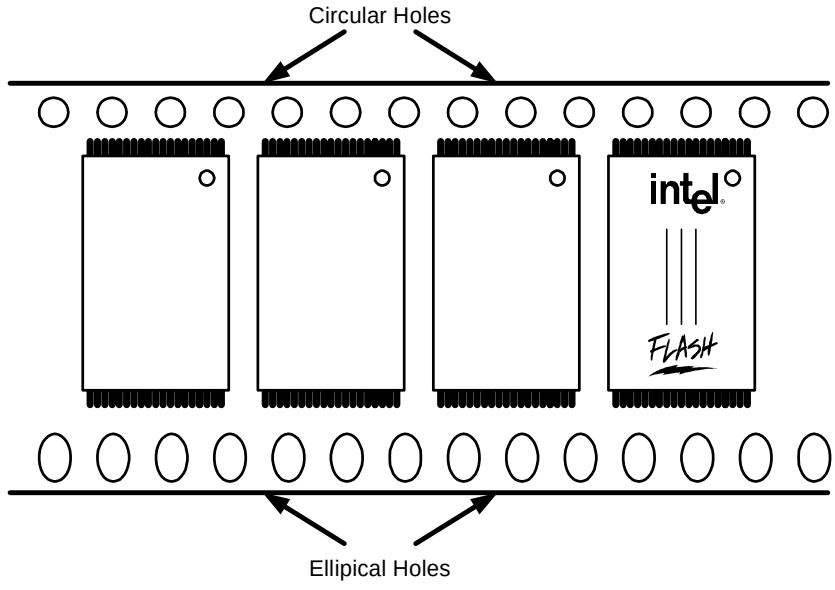


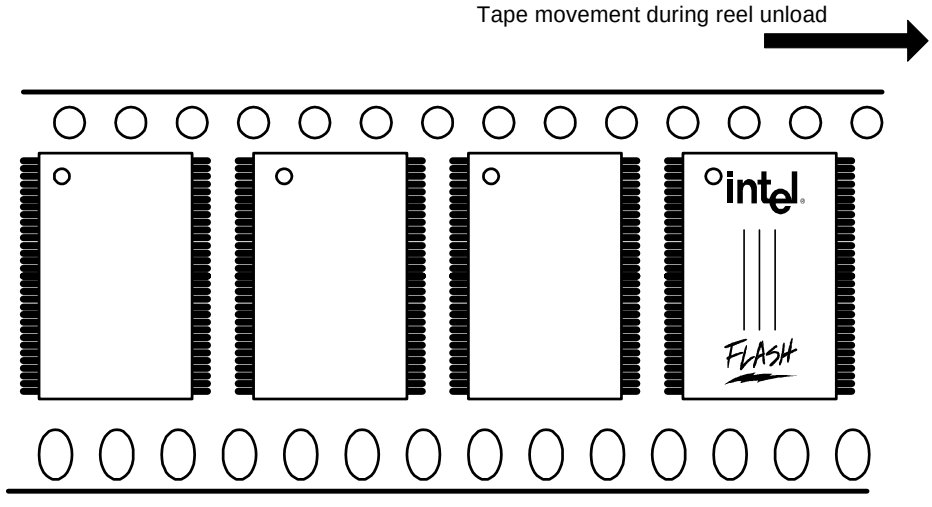
Figure 7-7. SOP Carrier Tape and Reel Dimensions

Table 7-5. SOP Carrier Tape and Reel Dimensions

Symbol	mm
A Max	330
D Max	20.2
W2 Max TSOP and SSOP	38.4
W2 Max PSOP and SSOP	50.4



32-L, 40-L, 48-L, 56-L TSOP



44-L PSOP and 56-L SSOP

Fig7-9

Figure 7-8. SOP Tape and Reel Orientation

7.1.5. PSOP Tubes

Intel's 44-lead PSOP products are shipped in 20-inch long, anti-static, ESD protected plastic shipping tubes, with 17 units per tube. The tube dimensions are shown in Figure 7-9.

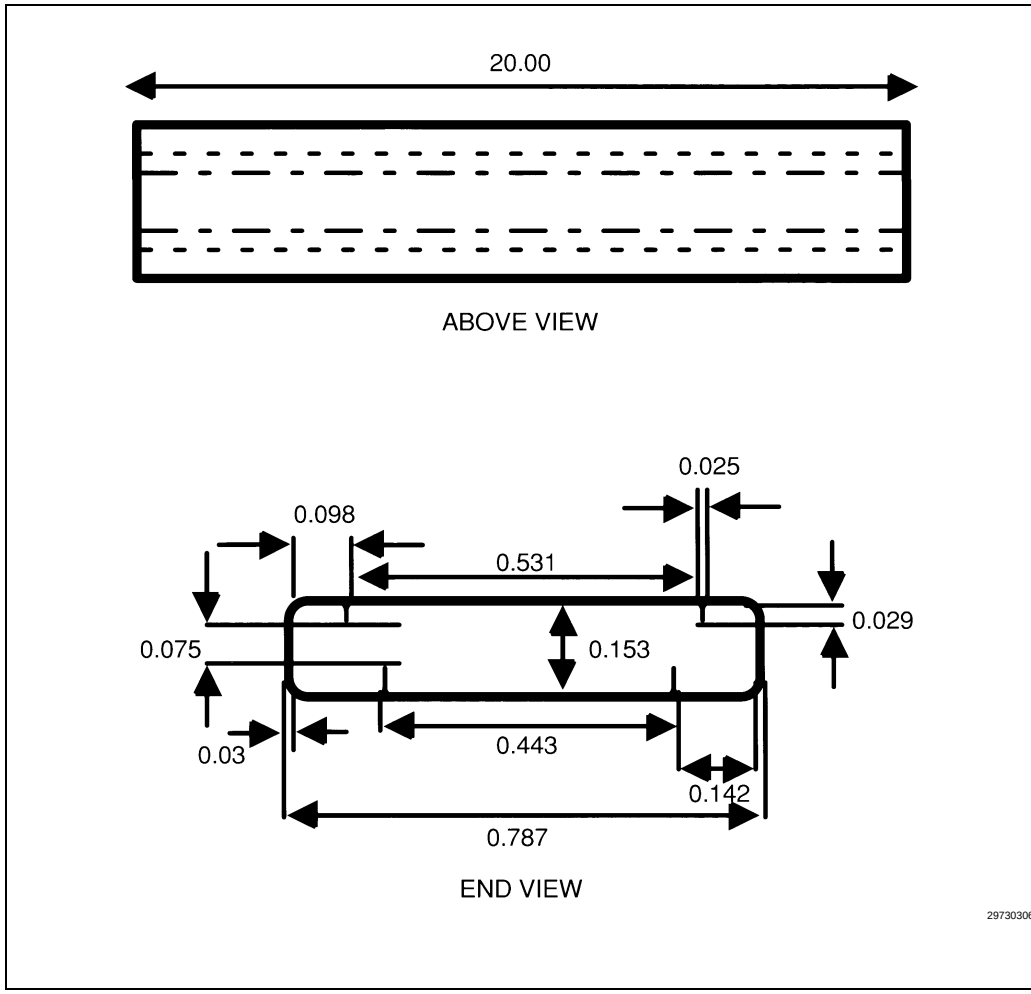


Figure 7-9. 44-Lead PSOP Shipping Tube

7.2. SOP PACKAGING REQUIREMENTS

SOP MOISTURE CONSIDERATIONS

Intel's family of Small Outline Packages (SOP) demonstrate excellent reliability performance. Absorption and desorption kinetics of the packages have been designed to be superior to that of conventional plastic packages.

Intel, in line with the IPC revisions to IPC-SM-786 (currently in process), is classifying surface mount components into several levels of moisture sensitivity. Table 7.6 lists the 6 IPC levels of moisture sensitivity for surface mount components (SMCs). Note that all bins are based on exposure time and environment. The label on the moisture barrier bag (MBB) lists the Moisture Sensitivity Level and the allowable floor life. See Figure 7-12.

Intel ships moisture sensitive plastic surface mount components (PSMCs) in a dry state inside moisture barrier bags (MBBs). Once the barrier bag has been opened, Intel recommends that components be surface mounted and reflowed within the time indicated on the Moisture Barrier Bag label. This time is based on a manufacturing environment not more extreme than 30 °C/60%RH. If the component can not be mounted within this timeframe, they should be put into a dry storage environment immediately, or sealed into a MBB with fresh desiccant as soon as possible. In either case, the remaining allowable ambient exposure time must be reduced by the time the units were out of the MBB or dry storage environment.

Table 7-6. Moisture Sensitivity Classification Levels for SMCs

Level	Description	Floor Life (Out of Bag) at Board Assembly Site
1	Non-Moisture Sensitive	Unlimited at 30 °C/85% RH
2	Limited Moisture Sensitivity	1 Year at 30 °C/60% RH
3	Moisture Sensitive	1 Week at 30 °C/60% RH
4	Highly Moisture Sensitive	72 Hours at 30 °C/60% RH
5	Extremely Moisture Sensitive	48 Hours at 30 °C/60% RH
6	Bake Before Use	6 Hours at 30 °C/60% RH

REBAKING OF PSMCs

- **High Temp Bake.** If the HIC indicates that the contents of the MBB have expired, the components can be baked to desorb moisture. Two bake temperatures are recommended, High and Low temp. The higher temperature bake is 125 °C for 24 hours for thicker packages (≥ 2 mm). For packages <2 mm thickness, a 6-hour bake at 125 °C is sufficient. This requires that the components be removed from plastic shipping tubes, trays or tape and reel and placed in metal or high temperature plastic containers. Components should be handled carefully to avoid lead coplanarity problems or any other type of damage. After this bake, the units may be exposed to an environment not more extreme than 30 °C/60%RH for a maximum of the time specified on the label.
- **Low Temp Bake.** Intel has also identified a low temperature bake profile. It allows component moisture desorption in the original plastic shipping containers and, thereby, avoids possible damage to component leads that might be introduced through additional handling. The low temperature bake is a 192-hour dwell at 40 °C(+5 °C, -0 °C)/≤5%RH. Figure 7-10 shows the curves for moisture desorption in these conditions. After 192 hours, saturated components will desorb moisture down to a residual moisture level that will allow ambient exposure, up to the time specified on the label, in environments not more extreme than 30 °C/60%RH before the safe allowable moisture content of the package is exceeded. Note that the temperature of the bake is limited by the thermal stability of the device shipping containers. The shipping containers will not hold dimension at bake temperatures higher than 45 °C (40 °C +5, -0 as indicated).

  It is not advisable to store PSMC units at the low bake temperature longer than the time required to dry out the units for use in the reflow. Lengthy storage times at elevated temperatures can lead to problems with intermetallic formation between the lead frame material and the lead finish, increased oxidation of the lead finish which can contribute to added reflow and wetting problems, and extended elevated temperatures can cause the antistatic properties of the shipping media (tubes/tape and reel) to deteriorate.
- **Solderability Considerations/Number of Rebakes.** Solderability tests performed on PSMCs exposed to either bake cycle are the basis for Intel's recommendations and limits on the number of allowable bake cycles. PSMCs should not be baked more than once by the customer if using the high temperature bake of 125 °C for 24 hours. Following this guideline will limit the formation of Cu_6Sn_5 intermetallic and therefore, not promote solderability degradation. The low temperature bake of 40 °C for 192 hours does not require this restriction.

NOTE

Solderability work done on solder dipped (not plated) PLCCs.

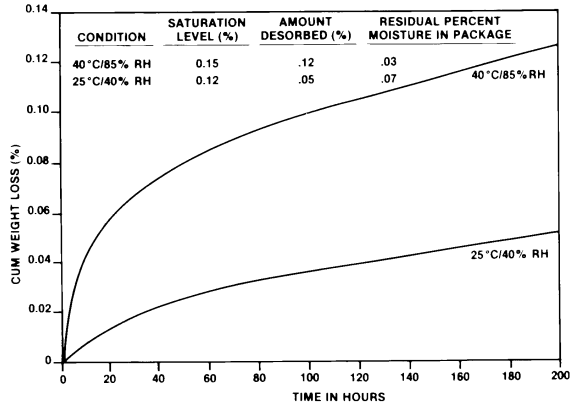


Figure 7-10. Saturated Component Weight Loss at Low Temperature

- Because components are baked in the shipping containers at the 40 °C bake—tubes, trays, or tape and reel—possible outgassing products as well as intermetallic formation impact on solderability were evaluated. Figure 7-11 is a "box plot" analysis of solderability measured by coverage of the leads in "number of squares." There is overlap in the distributions of, 1) the control units stored in metal trays, 2) units stored in plastic shipping containers and, 3) units baked in plastic shipping containers, therefore, there is no statistical difference between the treatments. No difference in solderability was observed after multiple rebakes at low temperature. Based on this data, there is no restriction on the number of times devices can be rebaked at the recommended low temperature before solderability is degraded beyond acceptable limits.

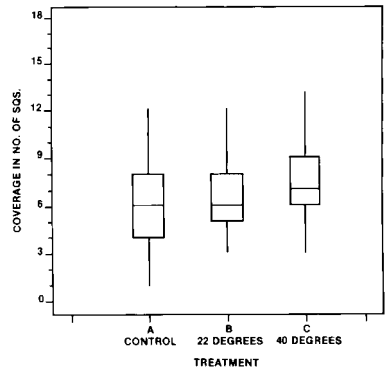


Figure 7-11. Solder Coverage versus Temperature

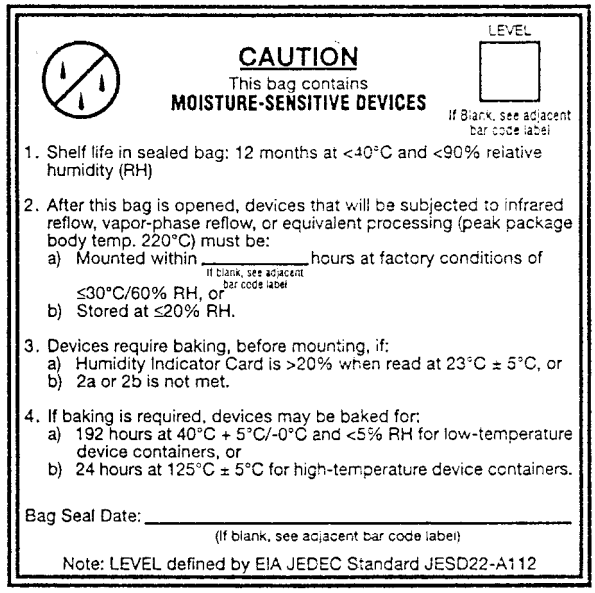


Figure 7-12. MBB "Caution Label"

PRECONDITIONING

Step 1: The devices are first baked at 125 °C, 6 hr--24 hr, followed by 5 cycles of T/C “B” to establish a baseline moisture level in all packages. This baseline is equivalent to sealing the components in moisture barrier bags.

Step 2: The components are then exposed to controlled humidity and temperatures for a given time (refer to Table 7.7). This step reflects the potential moisture intake of the component when moisture barrier bags are opened and left open for the amount of time marked on the bags.

Step 3: These moisture soaked components are then subjected to a typical IR/VPS reflow profile.

Step 4: The components are analyzed further for mechanical integrity and electrical performance.

Reliability data gathered after preconditioning, more accurately reflects the life expectancy in the final application in the field.

The following flowchart (Figure 7-13) indicates how SMT process stressing is comprehended in Intel's component reliability evaluations. User manufacturing processes not comprehended by this preconditioning flow should be discussed with Intel engineers.

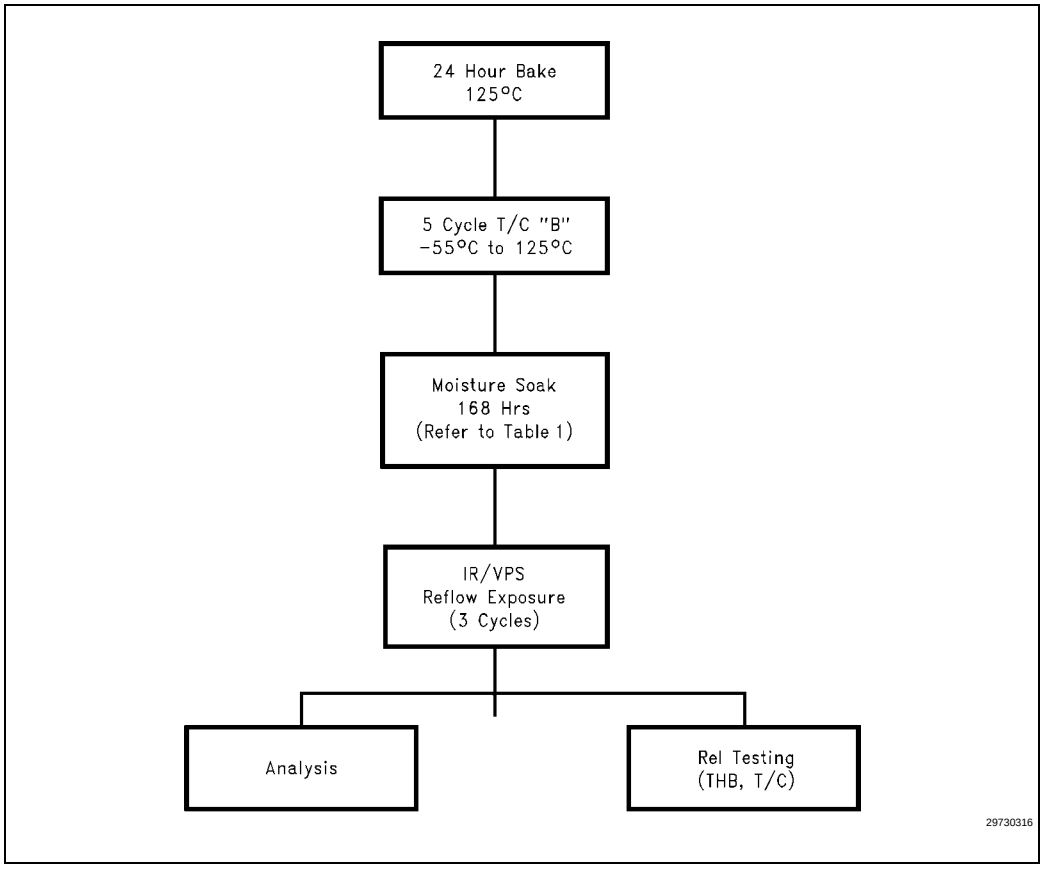


Figure 7-13. SOP Stress Process Flow

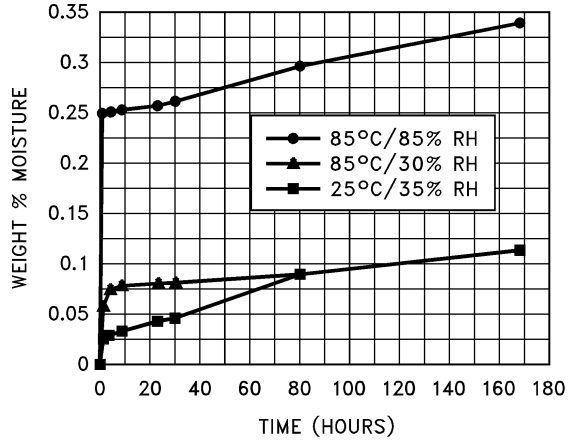
Table 7-7. Test Conditions Table

Level	At Board Assembly Site	°C/%RH	Time (Hrs)
1	Unlimited at 85% RH	85/85	168
2	1 Year at 30 °C / 60% RH	85/60	168
3	1 Week at 30 °C / 60% RH	30/60	216
4	72 hours at 30 °C / 60% RH	30/60	120
5	48 hours at 30 °C / 60% RH	30/60	96
6	Mandatory Bake: Bake before use, and once baked must be reflowed within the time limit specified on the label.	30/60	Time on Label

The results of preconditioning and the corresponding rel testing and analysis resulted in the following IPC/JEDEC moisture sensitivity levels for Intel's small outline packages. See Table 7.8.

Table 7-8. SOP Moisture Reliability Levels

Package	Pins	IPC/JEDEC Level
TSOP	32	2
	40	2
	48	3
	56	2
PSOP	44	3
SSOP	56	2



NOTES:

In high humidity conditions (85 °C/85% RH, 85 °C/30% RH), most of the weight gain occurs in the initial four hours.

At A/C environment (25 °C/35% RH), most of the weight gain occurs in the initial 80 hours.

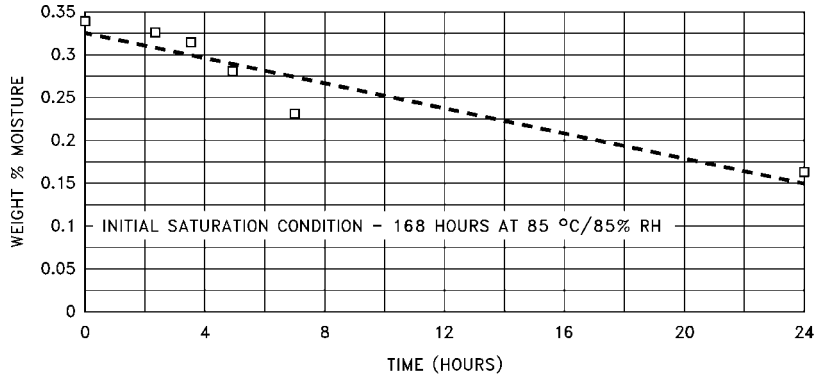
MOISTURE BARRIER BAG IMPLICATIONS:

Within a 48-hour window, the package may reach a 0.27% moisture level in extremely humid environments. Under normal conditions, it may gain as much as 0.1% moisture.

Six months of storage out of the bag may allow as much as 0.1% moisture under 25 °C/35% RH.

After opening the bag, the unit may gain moisture to between the 0.1% to 0.34% level if left indefinitely in a high humidity environment.

Figure 7-14. TSOP Moisture Absorption by Weight

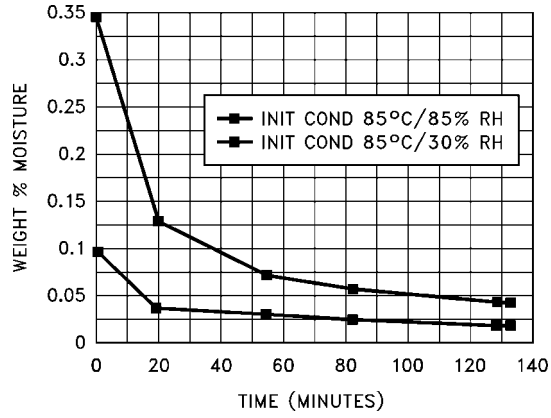


NOTES:

A saturated/soaked package retains significant amounts of moisture for the first 5 hours.

All VPS/IR reflow exposures for preconditioning application were performed within a two hour window from saturation.

Figure 7-15. TSOP Moisture Desorption at 25 °C



NOTES:

During bake, most of the moisture is lost within the initial 20 minutes. In contrast, a 68-lead PLCC loses similar amounts of moisture in 12 hours.

SURFACE MOUNT IMPLICATIONS:

The package will lose significant amounts of moisture during preheat of VPS/IR.¶

A soaked package will be reasonably “dry” during the critical temperature exposures (220 °C—260 °C).¶

Figure 7-16. TSOP Moisture Desorption at 125 °C

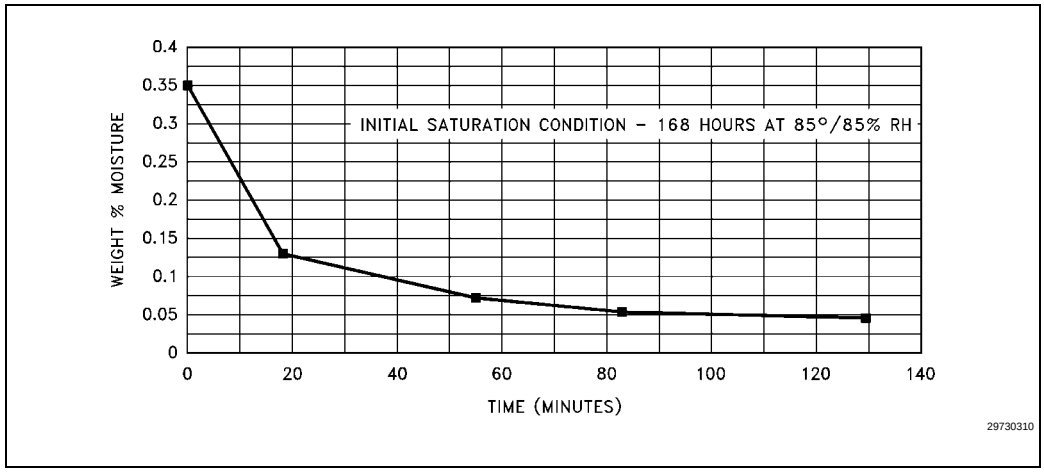


Figure 7-17. TSOP Desorption at 125 °C

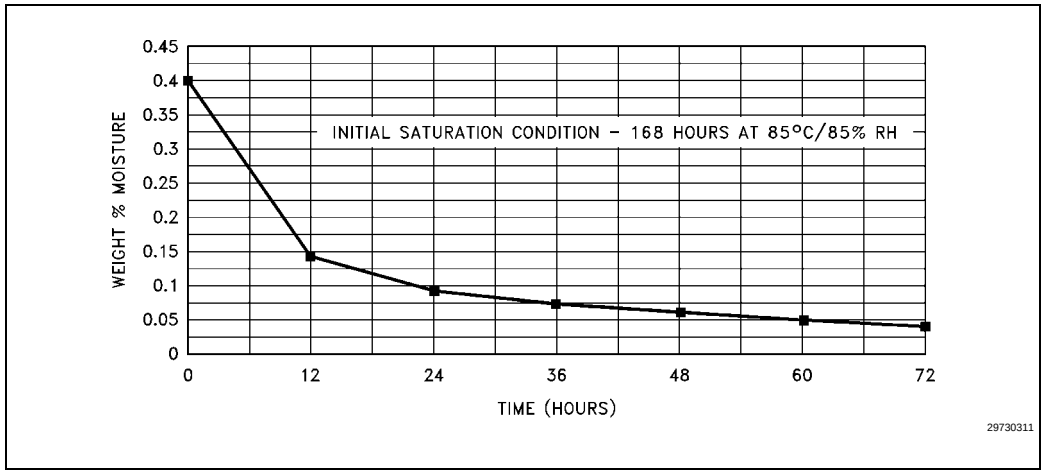


Figure 7-18. 68-Lead PLCC Desorption at 125 °C
(for comparison, note differences in time scale)

8

SOP SMT Assembly Considerations

CHAPTER 8
SOP SMT ASSEMBLY CONSIDERATIONS

Fine pitch SMT packages such as the 0.50 mm pitch TSOP package requires special assembly considerations. This chapter is intended as another tool to help you develop a manufacturable surface mount process. The following recommendations are not the only way to accomplish the task at hand. However, these recommendations document our best experiences in working with these fine pitch packages.

8.1. STORAGE AND HANDLING

Because the leads are closely spaced and the packages are extremely thin, special precaution must be taken to maintain package integrity. The storage trays are designed to secure the TSOP package in the cavity of the tray, preventing lead damage. The trays should not be moved without a top tray securing the components in the tray below it. An empty tray should be on the top, holding the first layer of components secure

Intel's tape and reel is designed to secure the SOP package in the cavity of the tape, preventing lead damage. However, care must be taken not to bend or twist the carrier tape.

8.2. SCREEN PRINTING

8.2.1. Solder Paste

To achieve an acceptable print and proper reflow characteristics, the proper solder paste must be chosen. The types of powders are defined in ANSI/IPC-SP819. The type powder used can vary depending upon the opening chosen in the stencil pattern. Type 3 or Type 4 powder are most commonly used in the assembly of the TSOP1.

8.2.2. Solder Volume

The control of the solder paste volume is important to eliminate solder bridging and an insufficient solder condition. The volume of solder paste required on a pad can be calculated using the Laplace Equation. Total solder joint volume for the TSOP lead has been calculated to be between 976 and 1280 cubic mils. Using a solder paste which is 90% metal by volume, the total calculated solder paste volume on a SOP pad should be between 1878 and 2461 cubic mils.

8.2.3. Solder Mask

A dry film solder mask should be used. The rough surface left behind by liquid films can entrap solder paste and lead to leakages.

8.2.4. Stencil

Understanding the limitations on printability of the solder paste, the solder paste volume requirements and the capability of the equipment being used, the design of the solder stencil can now be undertaken. To form an optimal solder joint and to avoid bridging between component leads, less solder paste volume needs to be deposited on the fine pitch lands than on the standard 50 mil pitch lands. A number of different stencil opening patterns have worked to achieve an acceptable print and not deposit excessive paste which would cause bridging.

One way to reduce the volume of solder paste is to reduce the thickness of the stencil beyond the standard 8 mil to 10 mil thickness for 50 mil pitch components. A “step down” stencil has been used that reduces the stencil thickness around the TSOP package, while maintaining the standard stencil thickness for the rest of the 50 mil pitch components. For TSOP, a stencil thickness of 6 mils is recommended.

The “staggered pad” is an approach where the stencil opening alternates between being printed on the top and the bottom half of the pad. This approach may eliminate the need to reduce the thickness of the stencil.

The stencil opening should be smaller than, or close to the land pad dimensions. See Figure 3.7 through Figure 3.9 for the suggested land pad diagrams for each package.

8.2.5. Vision System

The close pad spacing of the SOP package requires that the stencil align very accurately with the image on the printed circuit board. Because of the tolerances associated with the printed circuit board manufacturing process and the screen printers capability of positioning the printed circuit boards in the same location each time, a screen printer with a vision system may be necessary.

8.2.6. Squeegee

Particular attention must be paid to the squeegee on the screen printer. A squeegee blade with a higher hardness value may be necessary to assure a complete print and to avoid “scooping” in the 6 mil TSOP openings.

To aid in the success of the screen printing process it is recommended that all TSOP patterns be placed in one direction on the printed circuit board. The orientation of the land patterns should be parallel to the direction of the travel of the squeegee blade. This will also help prevent scooping of the solder paste out of the stencil aperture.

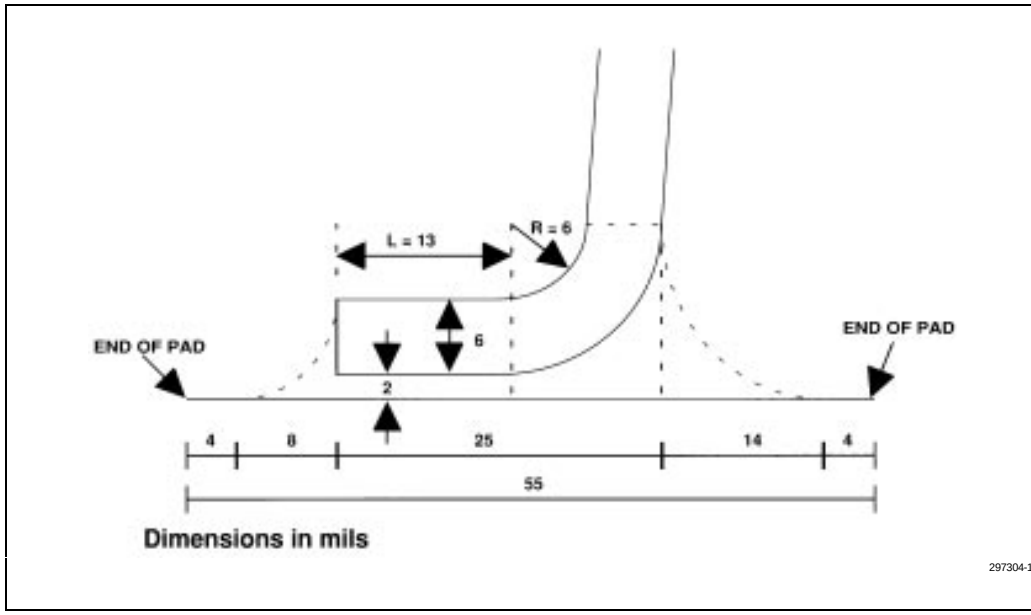


Figure 8-1. TSOP Lead Placement Close-Up View

8.3. PLACEMENT

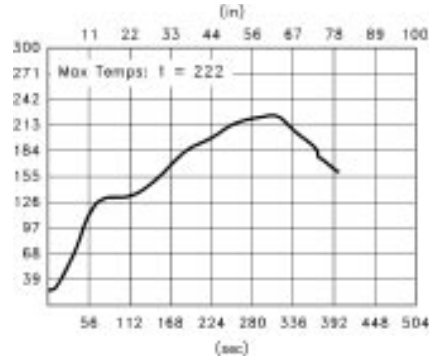
The placement equipment must have the required X, Y, and θ rotational accuracy to place the component within the specified "on pad" requirement. With the close spacing of the TSOP package, it is recommended that the component is placed with equipment which has both fiducial dot recognition vision and component vision.

Proper lead placement and solder joint fillet formation is shown in Figure 8-1.

8.4. CLEANING

Fine pitch packages such as the SOP have been historically cleaned using CFC-based chemicals. Because of the movement of the industry toward reduction of CFC use, alternative means to clean under the SOP package may need to be analyzed.

Typical IR Temperature Profile for 32-Lead TSOP



297304-2

Figure 8-2. IR Characteristics Typical Profile

8.5. IR FURNACE

A suggested IR furnace profile is shown in Figure 8-2. This figure shows a typical example of the IR profile. It is not intended to be an exact portrayal of an actual IR profile. The actual profile will vary depending upon the layout and type of other components on the board.

Peak profile temperatures in the 220°C to 225°C range ensure good eutectic solder joint formation with the Alloy 42 TSOP leadframe material.

8.6. DESIGN CONSIDERATIONS

The correct pad size and spacing for the SOP is important for a reliable and manufacturable design. Examples of lead to pad pass/fail alignment are shown in Figure 8-3 through Figure 8-5. Refer to Chapter 3 for land pad dimensions. The pad layout for the fine pitch part used will in part be determined by the process capabilities of the operation performing the assembly.

Fiducial targets are images in the copper of a printed circuit board that provide location data to the assembly equipment. A common fiducial target is a 0.050 inch in diameter round dot, with 0.15 inch diameter clearance area, free of soldermask. It is recommended that an additional fiducial target also be placed in the local area of the SOP land pattern. This local fiducial will provide improved resolution of the location of the land pattern which may result in improved SOP placement accuracy.

To aid in the success of the screen printing process it is recommended that all SOP patterns be placed in one direction on the printed circuit board. The orientation of the land patterns should be parallel to the direction of the travel of the squeegee blade. This will help prevent scooping of the solder paste out of the stencil aperture.

8.7. PASS/FAILURE MODE EXAMPLES

Figure 8-3 shows a SEM photo of good TSOP bond pad placement.

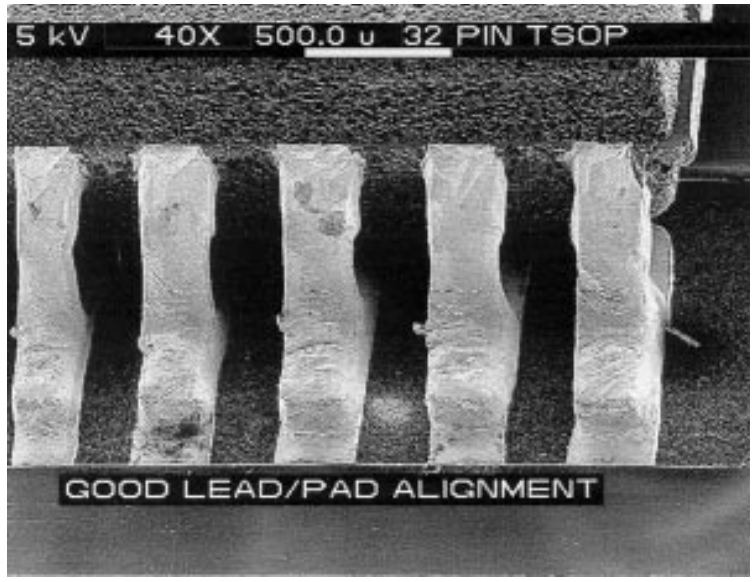


Figure 8-3. Example of Good Placement

Figure 8-4 shows a SEM photo of TSOP lead/pad misalignment.

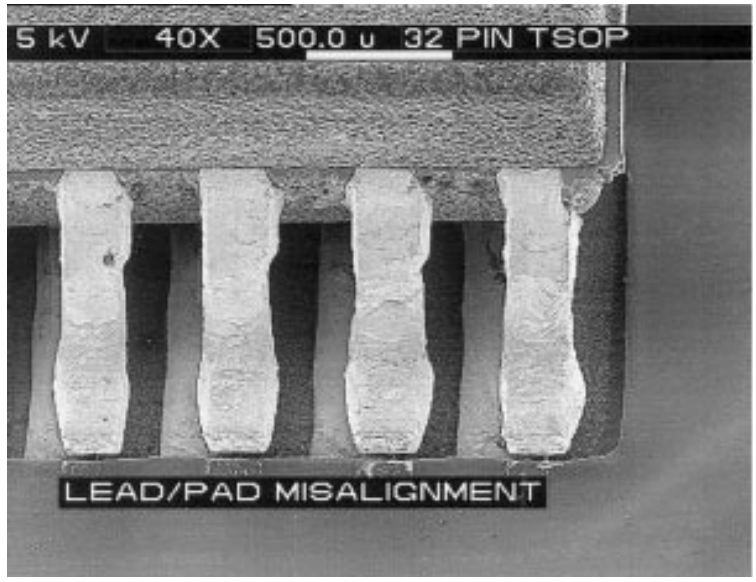


Figure 8-4. Example of Misalignment

Figure 8-5 shows a SEM photo of TSOP lead/pad lifting.

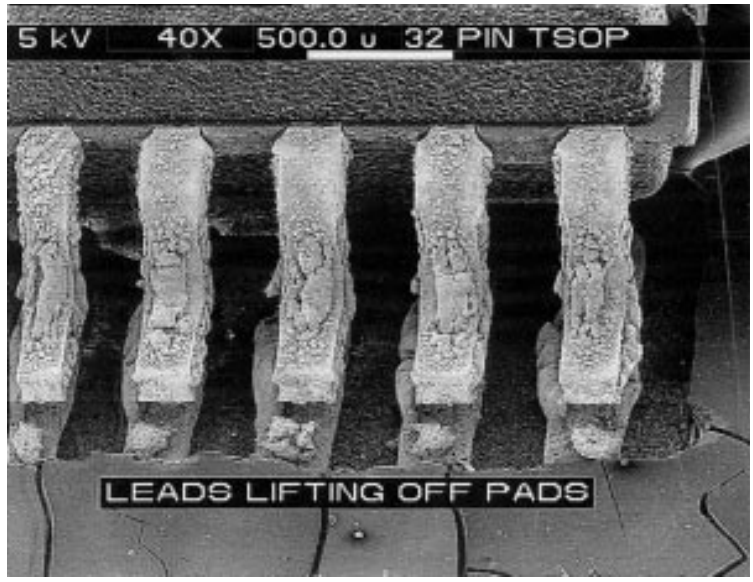


Figure 8-5. Example of Lifting

8.8. REWORK ISSUES

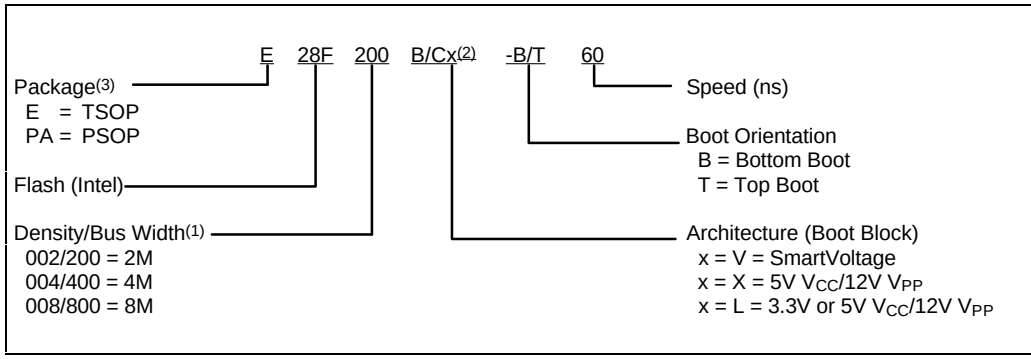
Intel does not recommend rework with fine pitch packages.

9

SOP Ordering Information

CHAPTER 9
SOP ORDERING INFORMATION

The nomenclature for ordering high-integration boot block flash memory products in TSOP and PSOP is as follows:



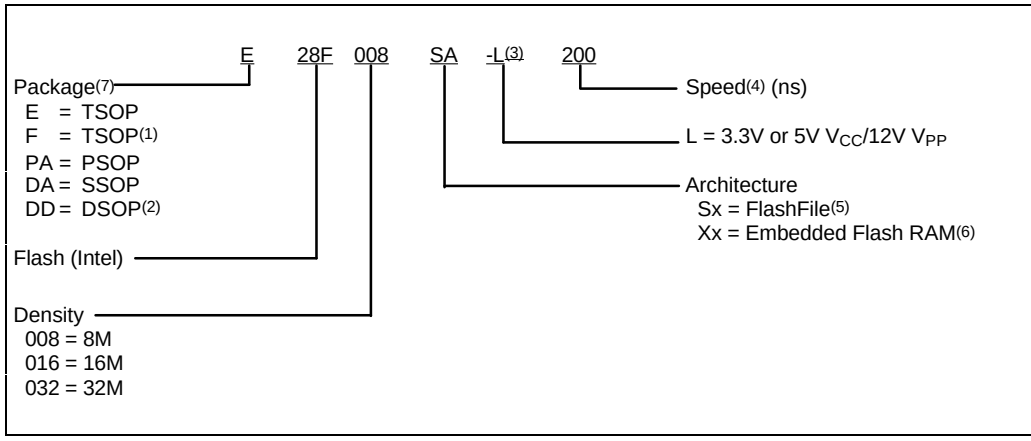
NOTES:

1. Parts numbered 28F002/004/008 have byte-wide data bus (offered in 40-Lead TSOP only); parts numbered 28F200/400/800 have user-selectable byte-wide or word-wide data bus capability.
2. The letter “C” indicates that E28200/400/800 devices are in 48-Lead TSOP so as not to be confused with E28F200/400/800 devices in 56-Lead TSOP.
3. Extended temp package identifiers: TB: PSOP, TE: TSOP “E”.

Examples:

40-Lead TSOP	44-Lead PSOP	48-Lead TSOP	56-Lead TSOP
E28F004BV-B60	PA28F400BV-B60	E28F400CV-B60	E28F400BV-B60
E28F004BV-T60	PA28F400BV-T60	E28F400CV-T60	E28F400BV-T60

The nomenclature for ordering high-density FlashFile memory or high-performance embedded Flash RAM products in TSOP, SSOP, Dual-Die TSOP and PSOP is as follows:



NOTES:

1. F = Reverse Pinout TSOP.
2. DSOP = Dual-Die TSOP.
3. L = a factory voltage screen for 3.3V V_{CC} capability; only applicable to 28F008SA.
4. On 28F016XS, speed indication means period of maximum CLK input frequency in nanoseconds.
5. SV incorporates SmartVoltage technology, SA does not.
6. x = S = synchronous pipelined interface; x = D = main memory (DRAM-like) interface.
7. Extended package identifiers: TB: PSOP, DT: SSOP, TE: TSOP "E".

Examples:

40-Lead TSOP	44-Lead PSOP	56-Lead TSOP	56-Lead SSOP	56-Lead DDTSOP
E28F008SA-85	PA28F800SA-85	E28F016SA-70	DA28F016SA-70	DD28F032SA-70
F28F008SA-85				

TSOP and SSOP product is shipped in trays or in Tape and Reel. PSOP product is shipped in tubes, trays, and tape and reel. Please refer to Chapter 7, *SOP Handling*, for more information on shipping formats and ordering quantities.

10

References and Additional Information

CHAPTER 10
REFERENCES AND ADDITIONAL INFORMATION

The following documents can be obtained through the Intel Customer Literature ordering department. Please reference the order numbers given below.

Intel Memory Products Handbook	Order Number 210830
Intel Packaging Handbook	Order Number 240800
Intel Surface Mount Packaging Guide	Order Number 240585
Prasad, Ray P. *Surface Mount Technology, Principles and Practice*, c1989, Van Nostrand Reinhold, New York	Order Number 555121

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641
1-(800)548-4725

A

SOP Support Tools

APPENDIX A
SOP SUPPORT TOOLS

Listing of third-party vendors in this appendix does not imply an endorsement by Intel Corporation of the vendors products and services. This list is not intended to be a complete list of equipment suppliers and should not be taken as such.

A.1. SOP MANUAL HANDLING AND PROGRAMMING PROCESS TOOLS/VIDEOS

Intel-Recommended Manual Handling and Programming Process for Small Outline Packages (SOP) Overview

Intent This overview provides quick reference for the Intel recommended manual handling and programming process for small outline packages.

Contents The table below details, in outline form, the type of information that can be found in the procedure.

How to order Intel's FaxBack* service:
1-800-628-2283 or (916) 356-3105 (US or Canada)
44(0)793-496646 (Europe)

FaxBack Document number 2291

Web site: www.intel.com
under the flash components info.

SOP handling/programming process instructional video:

Call Intel literature center: (800) 548-4725 or if outside of US or Canada, contact local sales office. OTI order number of video:

NTSC (USA, standard VHS format)	- 297684-001
PAL (Europe format)	- 297689-001
SECAM (Europe format)	- 297690-001

SOP total solutions video:

This video addresses the SOP manufacturing/assembly infrastructure based on testimonials from various business segments (assembly, distribution, tools, etc.).

NTSC (USA, standard VHS format)	- 297696-001
PAL (Europe format)	- 297697-001
SECAM (Europe format)	- 297698-001

Section	Contents
Training Video	Training Video is available which covers this entire process and provides examples of procedures and explanations of processes.
Manual Programming Process	Details programming specific items such as device placement into sockets, handling, label installation, quality monitor process, and manual/semi-automated lead inspection.
Packing Procedures	Reviews tray packing/un-packing procedures as well as tape-in-tube for small quantity shipments.
Handling Procedures	Covers handling SOP in trays from receiving to shipping and all the steps in between including, tray handling, desiccant bagging, bent leads, lead inspection, work station layout, ESD and handling precautions, tray strapping, and vacuum wand information.
Recommended Materials	Outlines 3 main tables on recommended materials such as vacuum wand information, process related equipment, and tray/tape-in-tube packaging materials.
Sourcing Information	Table provides contact information for all recommended materials.
Process Update Section	Provides a quick reference for any process related updates or issues.

A.2. SOP PROGRAMMING ADAPTER SUPPLIERS

Emulation Technology, Inc.
2344 Walsh Ave., Bldg. F
Santa Clara, CA 95051
(408) 982-0660

Product(s)	Package	Board/ Configuration	Vendor Part Number	Spreadsheet Code(1)
E28F016XS	56-lead TSOP	48 DIP (x16)	AS-56-48-02TS-6YAM-S (Rev.B) (2)	3rd Party 48x16
		40 DIP (x8)	AS-56-40-04TS-6YAM-S (Rev.B) (2)	3rd Party 40x8
E28F016XD	56-lead TSOP	40 DIP (x16)	AS-56-40-05TS-6YAM-S (3)	3rd Party
DD28F032SA E28F016SA/SV	56-lead TSOP	48 DIP (x16)	AS-56-48-01TS-6YAM-S (Rev.B) (4)	3rd Party 48x16
		44 DIP (x16)	AS-56-44-03TS-6YAM-S (Rev.B) (4)	3rd Party 44x16a
		40 DIP (x8)	AS-56-40-03TS-6YAM-S (Rev.B) (4)	3rd Party 40x8
E28F016SA/SV	56-lead TSOP	44 DIP (x16)	AS-56-44-02TS-6YAM-S (Rev.B) (4)	3rd Party 44x16
DA28F016SA/SV	56-lead SSOP	48 DIP (x16)	AS-56-48-01SS-6TI (5)	3rd Party 48x16
		44 DIP (x16)	AS-56-44-02SS-6TI (5)	3rd Party 44x16a
		40 DIP (x8)	AS-56-40-01SS-6TI (5)	3rd Party 40x8
		44 DIP (x16)	AS-56-44-01SS-6TI (5)	3rd Party 44x16
PA28F008SA	44-lead PSOP	40 DIP (x8)	AS-44-40-03S-6YAM (6)	3rd Party
E28F008SA	40-lead TSOP	40 DIP (x8)	AS-40-40-01TS-6YAM-S (6)	3rd Party
F28F008SA	40-lead TSOP (reverse pinout)	40 DIP (x8)	AS-40-40-01TS-6YAM-R (6)	3rd Party
E28F800CV E28F400CV E28F200CV	48-lead TSOP	44 DIP (x8/16)	AS-48-44-01TS-6WEL-S (7)	3rd Party 44
		40 DIP (x8)	AS-48-40-02TS-6WEL-S (7)	3rd Party 40-004
E28F400CV E28F200CV	48-lead TSOP	40 DIP (x8/16)	AS-48-40-01TS-6WEL-S (7)	3rd Party 40x16
E28F400BV/X/L E28F200BV/X/L	56-lead TSOP	44 DIP (x8/16)	AS-56-44-01TS-6YAM-S (Rev.B) (8)	3rd Party 44
		40 DIP (x8)	AS-56-40-02TS-6YAM-S (Rev.B) (8)	3rd Party 40-004
		40 DIP (x8/16)	AS-56-40-01TS-6YAM-S (Rev.B)	3rd Party 40x16

SOP Programming Adapter Suppliers (Continued)

Product(s)	Package	Board/ Configuration	Vendor Part Number	Spreadsheet Code(1)
PA28F800BV PA28F400BV/X/L PA28F200BV/X/L	44-lead PSOP	44 DIP (x8/16)	AS-44-44-01S-6YAM (Rev.B) (9)	3rd Party 44
		40 DIP (x8)	AS-44-40-05S-6YAM (Rev.B) (9)	3rd Party 40-004
PA28F400BV/X/L PA28F200BV/X/L	44-lead PSOP	40 DIP (x8/16)	AS-44-40-04S-6YAM (Rev.B) (9)	3rd Party 40x16
E28F008BV E28F004BV/X/L E28F002BV/X/L	40-lead TSOP	40 DIP (x8)	AS-40-40-02TS-6YAM-S (Rev.B) (10)	3rd Party
E28F001BX E28F020 E28F010	32-lead TSOP	32 DIP (x8)	AS-32-32-01TS-6YAM-S (11)	3rd Party
F28F020 F28F010	32-lead TSOP (reverse pinout)	32 DIP (x8)	AS-32-32-01TS-6YAM-R (11)	3rd Party
N28F020 N28F010 N28F512 N28F256A	32-lead PLCC	32 DIP (x8)	AS-32-32-01P-6YAM (11)	3rd Party

California Integration Coordinators, Inc.
656 Main St.
Placerville, CA 95667
(916) 626-6168

Product(s)	Package	Board/ Configuration	Vendor Part Number	Spreadsheet Code(1)
E28F016XS	56-lead TSOP	48 DIP (x16)	CIC-56TS-48D-B6-YAM-S (Rev.2) (2)	3rd Party 48x16
		40 DIP (x8)	CIC-56TS-40D-D6-YAM-S (Rev.2) (2)	3rd Party 40x8
E28F016XD	56-lead TSOP	40 DIP (x16)	CIC-56TS-40D-E6-YAM-S (3)	3rd Party
DD28F032SA E28F016SA/SV	56-lead TSOP	48 DIP (x16)	CIC-56TS-48D-A6-YAM-S (Rev.2) (4)	3rd Party 48x16
		44 DIP (x16)	CIC-56TS-44D-C6-YAM-S (Rev.2) (4)	3rd Party 44x16a
		40 DIP (x8)	CIC-56TS-40D-C6-YAM-S (Rev.2) (4)	3rd Party 40x8
E28F016SA/SV	56-lead TSOP	44 DIP (x16)	CIC-56TS-44D-B6-YAM-S (Rev.2) (4)	3rd Party 44x16
DA28F016SA/SV	56-lead SSOP	48 DIP (x16)	CIC-56SS-48D-A6-TI (5)	3rd Party 48x16
		44 DIP (x16)	CIC-56SS-44D-B6-TI (5)	3rd Party 44x16a
		40 DIP (x8)	CIC-56SS-40D-A6-TI (5)	3rd Party 40x8
		44 DIP (x16)	CIC-56SS-44D-A6-TI (5)	3rd Party 44x16
PA28F008SA	44-lead PSOP	40 DIP (x8)	CIC-44PS-40D-A6-YAM (6)	3rd Party
E28F008SA	40-lead TSOP	40 DIP (x8)	CIC-40TS-40D-A6-YAM-S (6)	3rd Party
F28F008SA	40-lead TSOP (reverse pinout)	40 DIP (x8)	CIC-40TS-40D-A6-YAM-R (6)	3rd Party
E28F800CV E28F400CV E28F200CV	48-lead TSOP	44 DIP (x8/16)	CIC-48TS-44D-A6-WEL-S (7)	3rd Party 44
		40 DIP (x8)	CIC-48TS-40D-B6-WEL-S (7)	3rd Party 40-004
E28F400CV E28F200CV	48-lead TSOP	40 DIP (x8/16)	CIC-48TS-40D-A6-WEL-S (7)	3rd Party 40x16
E28F400BV/X/L E28F200BV/X/L	56-lead TSOP	44 DIP (x8/16)	CIC-56TS-44D-A6-YAM-S (Rev.2) (8)	3rd Party 44
		40 DIP (x8)	CIC-56TS-40D-B6-YAM-S (Rev.2) (8)	3rd Party 40-004
		40 DIP (x8/16)	CIC-56TS-40D-A6-YAM-S (Rev.2) (8)	3rd Party 40x16

SOP Programming Adapter Suppliers (Continued)

Product(s)	Package	Board/ Configuration	Vendor Part Number	Spreadsheet Code(1)
PA28F800BV PA28F400BV/X/L PA28F200BV/X/L	44-lead PSOP	44 DIP (x8/16)	CIC-44PS-44D-A6-YAM (Rev.2) (9)	3rd Party 44
		40 DIP	CIC-44PS-40D-C6-YAM (Rev.2) (9)	3rd Party 40-004
PA28F400BV/X/L PA28F200BV/X/L	44-lead PSOP	40 DIP (x8/16)	CIC-44PS-40D-B6-YAM (Rev.2) (9)	3rd Party 40x16
E28F008BV E28F004BV/X/L E28F002BV/X/L	40-lead TSOP	40 DIP (x8)	CIC-40TS-40D-B6-YAM-S (Rev.2) (10)	3rd Party
E28F001BX E28F020 E28F010	32-lead TSOP	32 DIP (x8)	CIC-32TS-32D-A6-ENP-S (11)	3rd Party
F28F020 F28F010	32-lead TSOP (reverse pinout)	32 DIP (x8)	CIC-32TS-32D-A6-ENP-R (11)	3rd Party
N28F020 N28F010 N28F512 N28F256A	32-lead PLCC	32 DIP (x8)	CIC-32PL-32D-A6-YAM (11)	3rd Party

NOTES:

1. Spreadsheet applies to Lotus*-123 documents or files that track programming support for the devices above. Both minimum software revision and all vendor hardware specifics are documented in the spreadsheets. Code applies to the adapter or sub-adapter columns in the spreadsheet, specifying the correct adapter for a given PROM programmer model when more than one adapter for a particular device/package is available. These spreadsheets can be found on Intel's FaxBack system and BBS.

Product Covered	FaxBack Doc #	Product Covered	BBS Filename
28F016XS 28F016XD	2251 2253	Embedded Flash RAM	FRAMPGM.EXE
28F032SA 28F016SA/SV 28F008SA	2222 2213 2582	FlashFile™ Memory Technology	FFILEPGM.EXE
28F800/008 28F400/004 28F200/002 28F001BX	2285 2581 2580 2579	Boot Block Flash Memories	BOOTPGM.EXE
28F020 28F010 28F512 28F256A	2578 2577 2576 2575	Bulk Flash Memories	BULKPGM.EXE

Adapter specification sheets can be found on FaxBack via the following document numbers:

2. 2252
3. 2254
4. 2226
5. 2259
6. 2225
7. 2262
8. 2261
9. 2260
10. 2224
11. 2223

*Other brands and names are property of respective owners.

A.3. SOP DISTRIBUTION PROGRAMMING SUPPORT

Distributors offer pre-programming of PROM devices. The level of automation and volume capability offered varies with each Distributor and their individual sites. Each of the distributors listed below offer SOP programming services. Information on their capability is available by contacting the following.

Flash Programming at USA Distribution Branches

ANTHEM	For location of appropriate branch call 1 (800) 8ANTHEM
ARROW	For location of appropriate branch call 1 (800) 777-ARRO
AVNET/HAMILTON	For location of appropriate branch and phone number call 1 (800) 332-8638
PIONEER-TECH	For location of appropriate branch and phone number call 1 (800) 227-1693
PIONEER-STANDARD	For location of appropriate branch call (512) 835-4000
WYLE ELECTRONICS	For location of appropriate branch call 1 (800) 414-4144

Flash Programming at Europe Distribution Branches

Firm	Address
BYTECH COMPONENTS	12A Cedarwood Chineham Business Park Crockford Lane Basingstoke Hants RG12 1RW England
AVNET ACCESS	Jubilee House Jubilee Road Letchworth Hertfordsire SG6 1QH England
ARROW MMD	3 Bennet Count Bennet Road Reading Berks RG2 OQX England
ARROW ELECTRONICS U.K. LTD.	Unit 11 Vestry Road Sevenoaks Kent TN14 5EU England
DATRONTECH	42–44 Birchett Road Aldershot Hants GU11 1LU England

Flash Programming at Europe Distribution Branches (Continued)

Firm	Address
AVNET NORTEC A/S	Postboks 1 23 N-1364 Hvalstad Norway
FARNELL ELECTRONIC SERVICES	Ankdammsgatan 32 Box 13 30 S-171 26 Solna Sweden
C2000 FINTRQNICS	Pyyntitle, 3 SF-00230 Espoo Finland
COMPUTER 2000 LLD	Zabeel Road PO Box 50818 Dubai United Arab Emirates
AVNET E2000 GMBH	Stahlgruberring 12 81829 Munich Germany
JERMYN CMBH	Im Dachssfueck 9 65549 Limburg Germany
PROELECTRON VERTRIEBS GMBH	Max-Planck-Str. 1 -3 63303 Dreieich Germany
ELBATEX AUSTRIA	Eitnergasse 6 A -1231 Vienna Austria
ELBATEX SWIZ	Hardstr. 7 CH-5430 Wettingen Switzerland
INDUSTRADE AG	Hertistr. 31 CH-8304 Wallisellen Switzerland
IMITEC	Zurichstrasse CH-8185 Winkel-Ruti
AVNET	79, Rue Pierre Semard F-92322 Chatillon France
TEKELEC	Cite des Bruyeres 5, Rue Carle Vernet BP 2 F-92310 Sevres France

Flash Programming at Europe Distribution Branches (Continued)

Firm	Address
ARROW ELECTRONIQUE	73 • 79 Rue des Solets Silic 585 F-94663 Rungis Cedex France
ARROW ATD	Albasanz, 75 E-28037 Madrid Spain
KONING EN HARTMAN	Energieweg 1 NL-2627 AP Delft Netherlands
INELCO DISTRIBUTION	Avenue des Croix de Guerre 94 B-1120 Bruxelles Belgium
EASTRONICS LTD	11, Rozanis Street P.O.B. 39300 Tel Aviv 61392 Israel
AVNET EMG	Via Novara 570 1-20100 Milano Italy
FARNELL SPA	Milanofiori Palazzo E5 1-20094 Assago (Milano) Italy
LASI ELECTRONICA	Viale Fulvio Testi, N.280 I-20126 Milano Italy
EMPA ELECTRONIC	Florya is Merkezi Besyol Londra Asfalti R-34630 Florya Istanbul Turkey
POULIADIS ASSOCIATES CORP.	Aristotelous St. 3 Sygrou Av. 150 GR-Athens 17671 Greece
EBE	PO Box 912-1222 Silverton 0127 178 Erasmus Street Mayerspark Pretoria 0184 South Africa
STINS COMAN	126 Pervomaiskaya St. Moscow 105203 Russia

Flash Programming at Europe Distribution Branches (Continued)

Firm	Address
KVASAR	Popudrenko Str. 52b 253078 Kiev Ukraine
MARVEL	Shalernaja (Voinova) St. 49 193015 St. Petersburg Russia
R-STYLE INVESTMENT LTD.	Vserossijsky Vystavochny Center (V.V.TS.) P.O. Box Nr. 46 129223 Moscow Russia

A.4. SOP INDEPENDENT PROGRAMMING HOUSES

Programming vendors offer third-party pre-programming of PROM devices. The level of automation and volume capability offered varies with each vendor. SOP programming support services are available from the following vendor:

A & J Assembly 125 Lewis Rd #24 San Jose, CA 95111 (408) 281-0100	**Programming Technology** 10015 Muirlands Blvd. Suite E Irvine, CA. 92718 (714) 454-0332
Integrated Programming, Inc. 2370 Qume Drive, Bldg. A San Jose, CA 95131 (408) 943-1155	**Source Electronics** 26 Clinton Dr. Hollis, New Hampshire 03049 (603) 595-2906
Mycroft 777 E. Brokaw Road San Jose, CA 95112 (408) 436-1566	**TeTech, Inc.** 549A Weddell Drive Sunnyvale, CA 94089 (408) 745-1133
Precision Programming 2088-A Walsh Ave. Santa Clara, CA 95050 (408) 988-6962	
Program Automation, Inc. 22706 Apen Street, Suite 308 El Toro, CA 92630 (714) 859-8200	

A.5. SOP SOCKET SUPPLIERS

Socket Vendors/Definitions

Intel Recommended Socket Vendors 12/05/94

Company	Address	Phone #	FAX #	Contact
Yamaichi	2235 Zanker Rd. San Jose, CA 95131	(408) 456-0797	(408) 456-0799	Al Muranaga
Texas Instruments	34 Forest St. Attleboro, MA 02703	(508) 699-5370	(508) 699-5339	Sal Rizzo
Meritec	1359 W. Jackson St. P.O. Box 8003 Painesville, OH 44077	(216) 354-2106	(216) 354-0687	Dick Wilkinson
Wells	1701 S. Main St. South Bend, IN 46613	(219) 287-5941	(219) 287-0356	John Hartstein
Enplas (call sales representative)	Tesco Int'l, Inc. 1825 S. Grant St. Suite 745 San Mateo, CA 94402	(415) 572-1683	(415) 341-1509	Valentino Yambing

DEFINITIONS:

Prototyping/Production socket—Typically used in R&D environment or early production run phases to facilitate removal/re-insertion of device for updating/fixing code. Characteristics include:

1) small form factor which can make device lock-in mechansim difficult to use
2) surface mountable
3) PCB land-pad layout similar/close to that of device
4) lower cost
5) low socket count [typically 10–100 insertions]

Burn-in/Programming/Test socket—Typically used for test and burn-in activities at a semiconductor manufacturer's facility, or a socketing solution for programming devices on a manually-operated PROM programmer or an automated handler. Characteristics include:

1) easy device insertion/removal via lock-in mechanism [usually because of larger form factor, especially in height]
2) high socketing count [typically ≥ 10,000 insertions]
3) thru-hole technology
4) normally more expensive than prototyping socket
5) usually higher operating temperature range than prototyping socket

SOCKET INFORMATION

Prototyping and Production Socket

Meritec Prototyping/Production Sockets

Package	Lead Count	Vendor	Part #	Codes
TSOP	32	Meritec	980020-32-0*	A, B
	40	Meritec	980020-40-0*	A, B
	48	Meritec	980020-48-0*	A, B
	56	Meritec	980020-56-0*	A, B
PSOP	44	Meritec	980021-44-0*	A, B
SSOP	56	Meritec	980022-56-0*	A, B

CODES:

A. Substitute part number's asterisk with "1" to exclude positioning pins, or "2" to include positioning pins.

B. 98002X version allows for permanent use of the socket in the design. It replaces the 98000X version (prototyping only version).

COMMENTS:

For pricing and availability please contact supplier.

Yamaichi Prototyping/Production Sockets

Package	Lead Count	Vendor	Part #	Codes
TSOP	32	Yamaichi	IC197-3202-2000	A
	40	Yamaichi	IC197-4004-2000	A
	48	Yamaichi	IC197-4807-2000	A
	56	Yamaichi	IC197-5606-2000	A
PSOP	44	Yamaichi	IC179-44600-500	
SSOP	56	Yamaichi	N/A	

CODES:

A. -2000 socket has metal cover, -2100 has a plastic section over center portion of cover

COMMENTS:

For pricing and availability please contact supplier.

SOCKET INFORMATION

Burn-In/Programming Socket

Package	Lead Count	Vendor	Part #	Codes
TSOP	32	Yamaichi	IC191-0322-001N IC191-0322-001	A, C, E A, B, E
		Enplas	OTS-32-0.5-03	C, E
	40	Yamaichi	IC191-0402-002N IC191-0402-002	A, C, E A, B, E
		Enplas	OTS-40-0.5-01	C, E
	48	Yamaichi	IC191-0482-004N IC191-0482-004	A, C, E A, B, E
		Wells	648-0482211-A31	E
	56	Yamaichi	IC191-0562-003N IC191-0562-003	A, C, E A, B, E
PSOP	44	Texas Instruments	CSP044-052	A, C, E, F
		Yamaichi	IC51-0442-1536	B, C, D
SSOP	56	Texas Instruments	CSP056-054	A, B, C, E

CODES:

A. Contains optical target.

B. With positioning pins.

C. Without positioning pins.

D. Clamshell socket.

E. Open-top socket.

F. Optimized for Copper PSOP leadframe; feet on alloy42 leadframe can be bent slightly downward.

COMMENTS:

For pricing and availability please contact supplier.

A.6. SOP PROGRAMMER AND HANDLER VENDORS

Programmer Vendor Addresses and Phone Numbers

Advantest Corp. Shinjuku-NS Bldg., 4-1 Nishi-Shinjuku 2-chome Shinjuku-ku, Tokyo 163 Japan +81(0)33-342-750	
Advantest AD (Takeda Systems) 77-1, Miyako Namekawa-Cyo, Hiki-Gun Saitama 355 Japan +81(0)49-356-4433	**Advantest America, Inc.** 2880 San Tomas Exprwy. #105 Santa Clara, CA 95051 (408) 970-9922
Advin Systems Inc. 1050-L E. Duane Ave. Sunnyvale, CA 94086 (800) 627-2456, (408) 243-7000	
Aval Data Corp. Information System Division Shinyuri-21 Bldg., 1-2-2 Mampukuji Asao-ku, Kawasaki-City Kanagawa 215 Japan +81(0)44-952-1322/1311	
B&C Microsystems Inc. 750 N. Pastoria Ave. Sunnyvale, CA 94086 (408) 730-5511	
BP Microsystems, Inc. 1000 N. Post Oak Rd. #225 Houston, TX 77055-7237 (800) 225-2101, (713) 688-4600	
Bytek Corp. 543 NW 77th St. Boca Raton, FL 33487 (800) 523-1565, (407) 994-3520	
Data I/O Corp. 10525 Willows Rd. NE Redmond, WA 98073 (800) 247-5700, (206) 881-6444	
Elan Digital Systems Ltd. Elan House, Little Park Farm Rd. Segensworth West, Fareham Hampshire PO15 5SJ United Kingdom +44(0)489-579799	**MSD3/Elan Systems US, Inc.** 365 Woodview Ave. #700 Morgan Hill, CA 95037 (408) 778-7267

Programmer Vendor Addresses and Phone Numbers (Continued)

Epro Corp. 3310 Victor Ct. Santa Clara, CA 95054 (408) 982-9707	
Logical Devices, Inc. 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766, (305) 428-6868	
Minato Electronics Inc. 4105, Minami Yamada-cho Kohoku-ku, Yokohama Kanagawa 223 Japan +81(0)45-591-5611	**Minato Electronics Inc.** 3628 Madison Ave. #5 North Highlands, CA 95660 (916) 348-6066
Needham's Electronics 4630-20 Beloit Dr. Sacramento, CA 95838 (916) 924-8037	
SMS North America, Inc. 17411 NE Union Hill Rd. #100 Redmond, WA 98052 (800) 722-4122, (206) 883-8447	**SMS Mikrocomputer Systeme GmbH** Im Grund 15, D-88239 Wangen, Germany +49(0)7522-97280
Stag Programmers Ltd. Silver Court, Watchmead Welwyn Garden City Herts AL7 1JT England +44(0)707-332148	**Stag Microsystems Inc.** 1600 Wyatt Dr. #3 Santa Clara, CA 95054 (800) 227-8836, (408) 988-1118
System General Corp. 1603-A S. Main St. Milpitas, CA 95035 (800) 967-4776, (408) 263-6667	**System General Corp.** 3F, #1 Alley 8, Lane 45, Bao Shing Rd. Shin Dian, Taipei, Taiwan ROC +886(0)2-917-3005

SOP PROGRAMMING HANDLERS

PSOP Automated Programming Handlers

Summary:

Programmer/handler solutions on the market for DIP and PLCC have been adapted for Intel's 44L PSOP (525 mil width). Two vendors offering this solution are:

Data I/O Corp.
Redmond, WA 98073
(800) 247-5700, (206) 881-6444

Kit #: PM 500-SOIC
Kit will convert Data I/O's DIP/PLCC Promaster series 3000, 7000 and 7500 programming systems.

Exatron Corp.
2842 Aiello Drive
San Jose, CA 95111
(800) Exatron, (800) 392-8766, (408) 629-7600

Kit Description: Change Over Kit for PSOP Devices Kit will retrofit to existing Model 5000 series handlers

TSOP, PSOP, and SSOP Automation Equipment Suppliers

The following matrix reflects some of the known automation equipment suppliers for SOP devices. It is not a complete list of all SOP automation suppliers. It does reflect currently known capabilities which are in the industry today.

Options listed are subject to change and systems may have additional options which are not included in this matrix. For further information, contact the manufacturer.

Equipment Type/Supplier	Options	Address	Phone Number
PROGRAMMING HANDLERS			
BP Microsystems	Tray, Tube, Tape/Reel, Laser Maker, Lead Scanner	1000 N. Post Oak Rd Houston, TX 77055-7237	(713) 688-4600
Data I/O	Tray, Tube, Tape/Reel, Laser Marker	10525 Willows Rd. P.O. Box 97046 Redmond, WA 98073-9746	(206) 881-6444
Exatron	Tube, Laser Marker	2842 Aiello Dr. San Jose, CA 95111	(408) 629-7600
SMS GmbH	Tray, Tube, Tape/Reel, Laser Marker, Lead Scanner	IM Grund 15 D-88239 Wangen i.A. Germany	49-7552-9728-21
Unmanned Solutions	Tray, Tube, Tape/Reel, Laser Marker, Lead Scanner	940 Auburn Court Fremont, CA 94538	(510) 656-4300
LEAD INSPECTION/CONDITIONING			
August Tech.	Semi-Auto	5237 Edina Industrial Blvd. Edina, MN 55439	(612) 820-0080
RVSI	In-Tray, Tape/Reel, Mark Inspect	425 Rabro Dr. E. Hauppauge, NY 11788	(516) 273-9700
Texas Instruments	In-Tray, Tape/Reel, Mark Inspect, Lead Conditioner	13020 Floyd Rd Dallas, TX 75243	(214) 917-4030
View	In-Tray, Mark Inspect	1650 N. Voyager Ave Simi Valley, CA 93063-3348	(805) 522-8439
TAPE/REEL			
Advantek	Tube	5801 Clearwater Minnetonka, MN 55343	(612) 938-6800
ISMECA	Tray, Tube, Laser Mark, Lead/Mark Vision, Test/Prog	Carlsbad, CA	(619) 931-1153
Systemation	Trays, Tube, Laser Mark, Lead/Mark/pin 1 vision Tape/reel	16805 W. Victor Rd. New Berlin, Wis 53151	(414) 785-1255
V-Tek	Tube, Counters	751 Summit Ave. Mankato, MN 56002-3104	(507) 387-2039

SOP Test Handler Vendors

Summary:

These types of handlers offer multiple output categories (greater than 2) and are based on pick and place technology. They can be configured to operate at a range of temperatures and are typically used in the final test manufacturing process. Vendors offering solutions are:

Delta Design, Inc.
5775 Kearney Villa Road
San Diego, CA 92123-1111
(619) 292-5000
FAX: (619) 277-7884

MCT
4635 N. First Street, Suite 101
San Jose, CA 95134
(408) 432-3200
FAX: (408) 432-8554

A.7. SOP MANUFACTURING EQUIPMENT SUPPLIERS

For a list of SOP manufacturing equipment suppliers, consult the directory entitled “North American Directory of Contract Manufacturers in Electronics” available from:

Directory of Contract Manufacturers
Directory Department
500 Howard Street
San Francisco, CA 94105
(415) 397-1881

Or, contract your local Intel Sales Office for more information.

A.8. SOP CUSTOM BOARD MANUFACTURING AND INTERPOSER MOUNTING

PSOP/TSOP interposers and general environmental (THB, 85°C/85% RH) and life test stress test (Burn-In and HVELT) boards are predesigned and readily available from the following vendor:

Echo Design and Development
1605 Remuda Lane
San Jose, CA 95112
(408) 436-1294
FAX: (408) 436-0824

Echo Design and Development

Product(s)	Package	Board	Vendor Part Number
E28F010 **E28F001BX** **E28F020**	32-Lead TSOP “E”	32-DIP	JC4047 Rev. 2
F28F010 **F28F020**	32-Lead TSOP “F”	32-DIP	JC4264
E28F008SA	40-Lead TSOP “E”	40-DIP	JC4046 Rev. 3
F28F008SA	40-Lead TSOP “F”	40-DIP	JC4268
E28F002BV/X **E28F004BV/X** **E28F008BV/X**	40-Lead TSOP “E”	40-DIP	JC4046 Rev. 3
PA28F008SA	44-Lead PSOP	40-DIP	JC4272
PA28F200BV/X **PA28F400BV/X** **PA28F800BV/X**	44-Lead PSOP	40-DIP	JC4276
E28F200CV **E28F400CV** **E28F800CV**	48-Lead TSOP	48-DIP	JC4890
E28F200BV/X **E28F400BV/X** **E28F800BV/X**	56-Lead TSOP “E”	56-DIP	JC4276
E28F016SA	56-Lead TSOP “E”	56-DIP	JC4275
DD28F032SA	56-Lead TSOP “DD”	56-DIP	JC4277

B

References

APPENDIX B
REFERENCES

Moisture Sensitivity of Thin Small Outline Packages. S. Golwalkar, P. Boysan, R. Foehringer, Intel Corporation. J. Jacobs, University of California at Berkeley. Proceedings of 41st ECTC, pp. 745-49 (1991).

Thin Film Cracking in Plastic Packages—Analysis, Model and Improvements. R. Foehringer, S. Golwalkar, S. Eskildsen, S. Altimari, Intel Corporation. Proceedings of 41st ECTC, pp. 759-65 (1991).

Role of Design Factors for Improving Moisture Performance of Plastic Packages. S. Altimari, S. Golwalkar, P. Boysan, R. Foehringer, Intel Corporation. Proceedings of 42nd ECTC, pp. 945-50 (1992).

Attachment Reliability Evaluation and Failure Analysis of Thin Small Outline Packages with Alloy 42 Leadframes. P. Boysan, S. Golwalkar, R. Foehringer, Intel Corporation. D. Noctor, F. Bader, A. Viera, AT&T Bell Laboratories. Proceedings of 43rd ECTC (1993).

Solder Joint Reliability of a Thin Small Outline Package. S. Golwalkar, P. Boysan, R. Surratt, R. Foehringer, Intel Corporation. J. Lau, D. Rice, S. Eramus, Hewlett-Packard Company. Proceedings of 43rd ECTC, pp. 519-32 (1993).

Experimental and Analytical Studies of 28-Lead Thin Small Outline Package (TSOP), Solder Joint Reliability. S, Golwalkar, P. Boysan, R. Surratt, Intel Corporation. J. Lau, S. Eramus, Hewlett-Packard Company. Transactions of the ASME, Journal of Electronic Packaging, pp. 169-76 (June 1992).

Advantages and Disadvantages of Thin Small Outline Package (TSOP) with Cu Gull-Wing Leads. S. Golwalkar, Intel Corporation. J. Lau, Hewlett-Packard Company. ASME International Electronic Packaging Conference, Binghampton, NY (September 1993).

Solution to Moisture Resistance Dehydration during Solder Reflow of Plastic Surface Mount Components. S. Golwalkar, Intel Corporation. Thermal Stress and Strain in Microelectronics Packaging, Van Nostrand Reinhold, edited by J. Lau, pp. 445-66 (1993).

C

SOP Standards Bodies

APPENDIX C
SOP STANDARDS BODIES

The following standards bodies provide specifications and/or documents concerning Integrated Circuit component packages, shipping media, and standard procedures for surface-mount, moisture-handling, etc. For more information, please contact the individual organizations below.

Electronics Industry Association (EIA)
and JEDEC Subcommittee
2001 Eye Street, NW
Washington, DC 20006
(202) 457-4930

American National Standards Institute
1430 Broadway
New York, NY 10008

Institute for Interconnecting and Packaging Electronic Circuits (IPC)
7380 North Lincoln Avenue
Lincolnwood, IL 60646
(312) 677-2850

Electronics Industry Association of Japan
Tokyo-Shokou-Kaigisho Building 5F
3-2-2 Marunouchi, Chiyoda-ku,
Tokyo, Japan 100
3-3211-2765